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Bachelor in Micro and Nanotechnologies Engineering

Design of Inverter Based CMOS Amplifiers in Deep Nanoscale Technologies

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“You have no responsibility to live up to what other people think you ought to accomplish. I have no responsibility to be like they expect me to be. It's their mistake, not my failing”

-Richard Feynman

Acknowledgments

Finishing this master thesis marks the closure of one chapter of my life and sets me up for another one. It is a very important mark for me that wouldn't be possible without the support of some people that I would like to show some appreciation to.

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Nano Dilemas, Tomás, Barroso, Filipe, Pereira, Nuno. It was several years of remarkably interesting conversations and dilemmas in that group, but the greatest victory goes to Nuno, who was able to stay in the group up until the end, we should have kicked him out.

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Abstract

In this work, it is proposed a fully differential ring amplifier topology with a deadzone voltage created by a CMOS resistor with a biasing circuit to increase the robustness over PVT variations.

The study focuses on analyzing the performance of the ring amplifier over process, temperature, and supply voltage variations, in order to guarantee a viable industrial employment in a 7 nm FinFET CMOS technology node for being used as residue amplifier in ADCs.

A ring amplifier is a small modular amplifier, derived from a ring oscillator. It is simple enough that it can quickly be designed using only a few inverters, capacitors, and switches. It can amplify with rail-to-rail output swing, competently charge large capacitive loads using slew-based charging, and scale well in performance according to process trends.

In typical process corner, a gain of 72 dB is achieved with a settling time of 150 ps. Throughout the study, the proposed topology is compared with others presented in literature showing better results over corners and presenting a faster response. The proposed topology isn't yet suitable for industry use, because it presents one corner significantly slower than the rest, namely process corner FF 125 °C, and process corner FS -40 °C with a small oscillation throughout the entire amplification period.

Nevertheless, it proved itself to be a promising technique, showing a high gain and a fast settling without oscillation phase, with room for improvement.

Keywords: Ring Amplifier; Inverter; Fully Differential; 7 nm CMOS.

Resumo

Neste trabalho, é proposta uma topologia de *ring amplifier* com a *deadzone* a ser criada através de uma resistência CMOS com um circuito de polarização para aumentar a robustez para as variações PVT.

O estudo foca-se em analisar a performance do *ring amplifier* nas variações de processo, temperatura e tensão de alimentação, de forma a garantir um uso viável em indústria na tecnologia de 7 nm FinFET CMOS, para ser usado como amplificador de resíduo em ADCs.

Um *ring amplifier* é um pequeno amplificador modular, derivado do *ring oscillator*. É simples o suficiente para ser facilmente projetado usando apenas poucos inversores, condensadores e interruptores. Consegue amplificar com *rail-to-rail output swing*, carregar grandes cargas capacitivas com carregamento *slew-based* e escalar bem em termos de performance de acordo com o processo.

No *typical process corner,* foi obtido um ganho de 72 dB com um tempo de estabilização de 150 ps. Durante o estudo, a topologia proposta é comparada com outras presentes na literatura mostrando melhores resultados *over corners* e apresentando uma resposta mais rápida. A topologia proposta ainda não está preparada para uso industrial uma vez que apresenta um *corner* significativamente mais lento que os restantes, nomeadamente, *process corner* FF 125 °C, e outro *process corner*, FS -40 °C, com uma pequena oscilação durante todo o período de amplificação.

Todavia, provou ser uma técnica promissora, apresentando um ganho elevado e uma rápida estabilização sem fase de oscilação, com espaço para melhoria.

Palavras-chave: *Ring Amplifier*; Inversor; *Fully Differential*; 7 nm CMOS.

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List of Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
AP	Anti-Parallel
BW	Bandwidth
CEMOP	Centro de Excelência de Optoeletrónica e Microeletrónica de Processos
CENIMAT	Centro de Investigação de Materiais
CM	Common Mode
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CS	Current Starved
DAC	Digital to Analog Converter
DC	Discrete Current
DZD	Deadzone Degenerated
DZ	Deadzone
ENOB	Effective Number of Bits
FD	Fully Differential
FF	Fast-Fast
FFT	Fast Fourier Transform
FinFET	Fin Field-Effect Transistor
FS	Fast-Slow
i3N	Institute for Nanostructures, Nanomodelling and Nanofabrication
IC	Integrated Circuit
I/O	Input/Output
MDAC	Multiplying Digital to Analog Converter
MOM	Metal-Oxide-Metal
NMOS	N-Type Metal Oxide Semiconductor
Opamp	Operational Amplifier
OS	Output Swing
OTA	Operational Transconductance Amplifier
PD	Pseudo Differential
PMOS	P-Type Metal Oxide Semiconductor
PVT	Process Voltage and Temperature
Ringamp	Ring Amplifier
SC	Switched Capacitor
SF	Slow-Fast
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SR	Slew-Rate
SS	Slow-Slow
THDDB	Total Harmonic Distortion in dB
TT	Typical-Typical
TSMC	Taiwan Semiconductor Manufacturing Company

UNINOVA	Instituto de Desenvolvimento de Novas Tecnologias
VCM	Common Mode Voltage
VDZ	Deadzone Voltage

List of Symbols

A_x	Gain of stage x
C_L	Load capacitance
C_{ox}	Gate dielectric capacitance per unit area
gm	Transistor's transconductance
I_{Ramp}	Current provided at the initial slewing phase
k	Boltzmann constant
L	Transistor's channel length
L_{min}	Transistor's minimum channel length
r_o	Output Impedance
T_{delay}	Total loop delay
$V_{DS,\,sat}$	Voltage between drain and source in saturation
V_{GS}	Voltage between gate and source
V_{Th}	Threshold voltage
W	Transistor's channel width
γ	Process dependent parameter
μ	Field-effect Mobility
Φ	Phase

1. Introduction

The semiconductor technology is facing a tremendous size scaling into the nanoscale regime, allowing more density on ICs. This increase in density in system-on-chip products requires an improved signal fidelity (i.e., increasing number of bits), leading to an increase in the requirements on ADCs or DACs, their support circuits, and high-speed I/O circuits. With reduced gate length, the intrinsic device speed has improved, but the intrinsic gain of devices has decreased. Degraded matching for minimum devices, worse flicker noise, and strong layout-dependency of parameters are some of the undesirable effects in analog devices. In addition, the supply voltage for nanoscale technologies has been reducing substantially, see Figure 1, all the way down to below 1 V, making the representation of analog information with a high signal-to-noise ratio (SNR) in the voltage domain significantly harder [1], [2]. The goal of this scaling is to allow a better performance by the digital circuits, since scaling minimum device length, L_{min}, directly improves digital processor and shorter devices are also faster and have less parasitic capacitance [1].

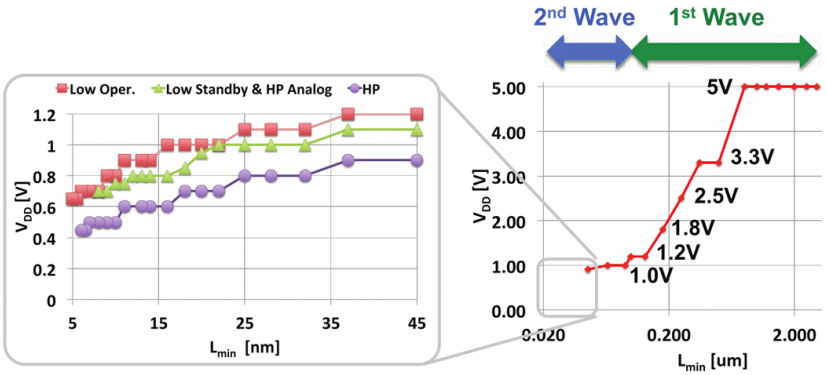

Figure 1 - Scaling of the core supply voltage vs. technology L_{min} [1].

One way to overcome the performance problems caused by scaling voltage supply is to use different strategies of scaling, as exposed in [1], like scaling with constant g_m/I or also scaling g_m/I. This strategy solves some problems, but not all of them, facing a barrier with topologies requiring devices in saturation mode, denominated in [1] as $V_{DS,sat}$ power wall, that has a strong effect on the output swing.

1.1 Motivation

Another way to overcome the aforementioned performance problems is to adopt different topologies. The predominant topology is still the closed-loop amplification with OTAs, operational transconductance amplifiers, having high power consumption, and poor scaling properties as limitations [3]–[8]. Highly cascoded single-stage topologies with special high-voltage supplies are used in high-speed designs instead of multi-stage Miller-compensated amplifiers, which are too slow [4], [5], [7]. Several open-loop amplification topologies have emerged as possible alternatives within this performance region [9]–[12]. All these structures present several attractive speed, noise, and efficiency advantages, but also require complex gain calibration and background monitoring.

Technology scaling is deliberately designed to favor the time-domain world of high-speed digital circuits. A truly scalable amplifier must operate in a way that implicitly uses the characteristics of scaled CMOS to its advantages, transforming potential weakness into inherent strengths [13]. In light of this, inverter-based amplifiers are considered as a solution, taking advantage of the digital world to overcome some of the current problems in analog amplifiers [14].

Several structures of inverter-based amplifiers were already studied, from single-stage inverter-based amplifiers [15]–[19], to two-stages inverter-based amplifiers [20], or even with three-stages [21], [22].

1.2 Objective

The goal of this work is to study a particular type of inverter-based amplifier, the ring amplifier, to be used in ADCs as residue amplifier. The study focuses on analyzing the ring amplifier's performance over process, temperature, and supply voltage variations, in order to guarantee a viable industrial employment in 7 nm FinFET CMOS technology node. This study was carried out as part of research for Xilinx's high speed ADCs development.

A ring amplifier is a small modular amplifier, derivative of a ring oscillator, which embodies all the essential elements of scaling [13]. It is simple enough that it can quickly be designed using only a few inverters, capacitors, and switches. It can amplify with rail-to-rail output swing, OS, competently charge large capacitive loads using slew-based charging, and scale well in performance according to process trends [13].

2. State of the Art

2.1 Inverter-Based Amplifier

To benefit from the advantages of the technology advances, there has been some development in inverter-based amplifiers. In literature, many different approaches can be found, depending on the final purpose. The following articles explore these approaches.

2.1.1 A Two-Stage Fully Differential Inverter Based Self-Biased CMOS Amplifier with High Efficiency

This article proposes a two cascaded inverter stages amplifier with both stages presenting approximately the same topology, Figure 2. The first stage, the input stage, consists of an inverter input pair connected to current sources. The transistors of the current sources bias and control the common mode level of the input stage. The output stage presents a very similar topology [20].

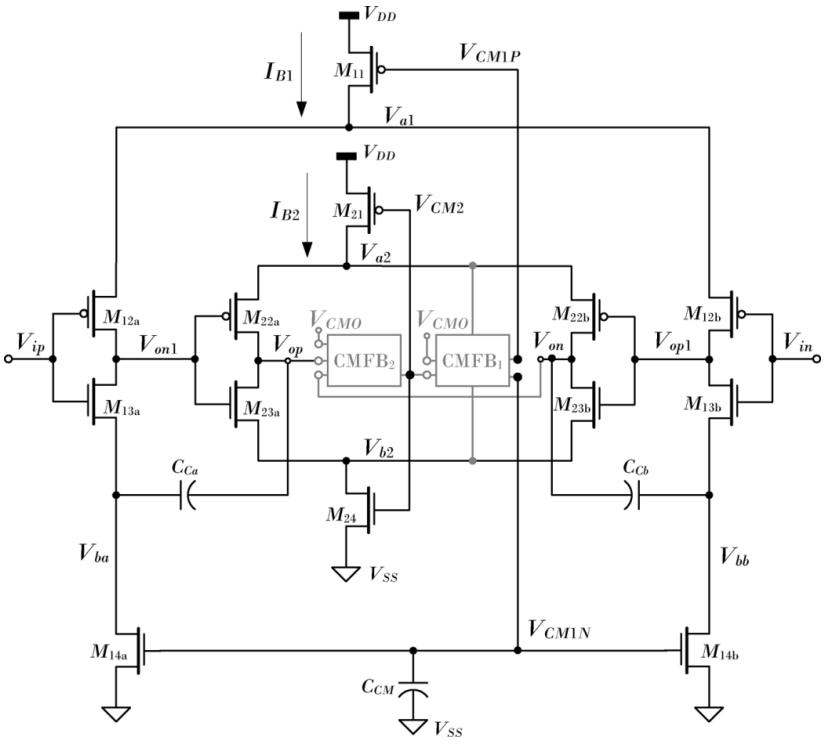

Figure 2 - Proposed topology of [20]. Two-stage inverter based self-biased amplifier.

The self-biasing presents several advantages, according to [20], such as simplifying the implementation by removing the biasing circuits, enabling circuits to be more PVT robust, and any mismatches and variations in circuit performance are attenuated.

The common mode feedback circuit shown in Figure 3 is responsible for biasing the whole amplifier and defining the CM control voltages for both stages. The CM level is controlled for the CMFB$_1$, formed by an inverter-based, that compares V_{CM2} with a constant voltage and generates the voltage that biases the input stage. The output CM level is adjusted by CMFB$_2$, a dedicated switch-capacitor CMFB circuit [20].

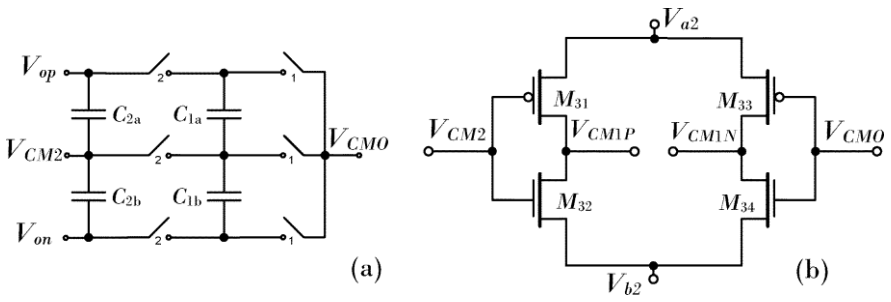

Figure 3 - Common mode feedback circuits presented in [20]. (a) SC network for output stage. (b) Continuous time CMFB circuit of input stage.

Self-biasing voltages V_{CM1P}, V_{CM1N} and V_{CM2} are connected to the main amplifier through feedback loops, thus, reducing the effects of PVT variations and the effects caused by differential-mode and CM input variations [20].

2.1.2 A 0.8-V 203-µW 98-dB DR Inverter-Based ΣΔ Modulator for Audio Applications

With the purpose of presenting a solution for low gain on traditional class-C, a gain-boost class-C inverter with on-chip body bias is proposed, Figure 4. On-chip body bias modules are introduced to compensate for the bandwidth and SR degradation, originated by slow process corner or low supply [16].

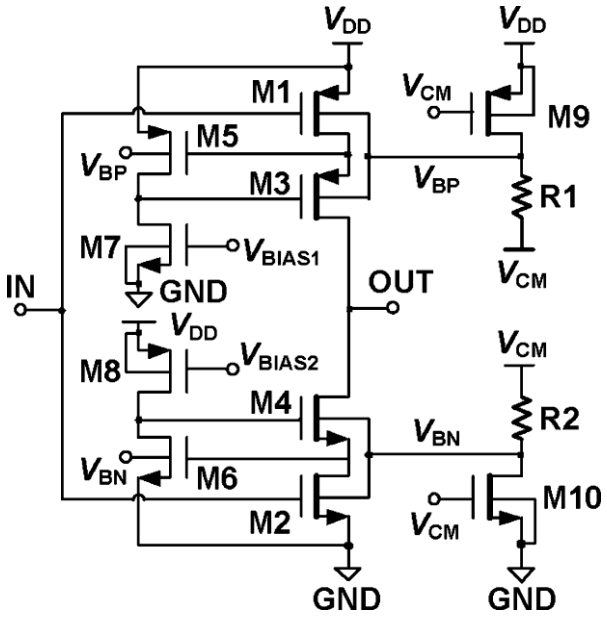

Figure 4 - Gain-boost class-C inverter with on-chip body bias [16].

The supply voltage for the inverter is chosen to be slightly lower than the sum of the threshold voltage of the input transistors. Both input transistors operate in a subthreshold region when the inverter input is around the CM voltage ($V_{CM}=V_{DD}/2$). Thus, the inverter behaves as a micro-power class-C amplifier [16].

The gain-boost module, M_5 to M_8, built up two current-voltage feedback loops together with M_3 and M_4. As a result, the output impedance and the DC gain of the gain-boost class C inverter are enhanced [16].

Due to its subthreshold characteristics and push-pull structure, the inverter is sensitive to process and V_{DD} variations, especially when slow process corner or low V_{DD}. The transconductance and the drain current of M_1 and M_2 reduce, and thus the BW and SR of the inverter are critically degraded, which may cause inverter-based circuits loss of function [16].

2.1.3 11 GHz UGBW Op-Amp with feed-forward Compensation Technique

A three stage cascaded inverter-based amplifier with feed-forward compensation technique is presented in [21], Figure 5. A normally unstable structure is stabilized by the feed-forward compensation.

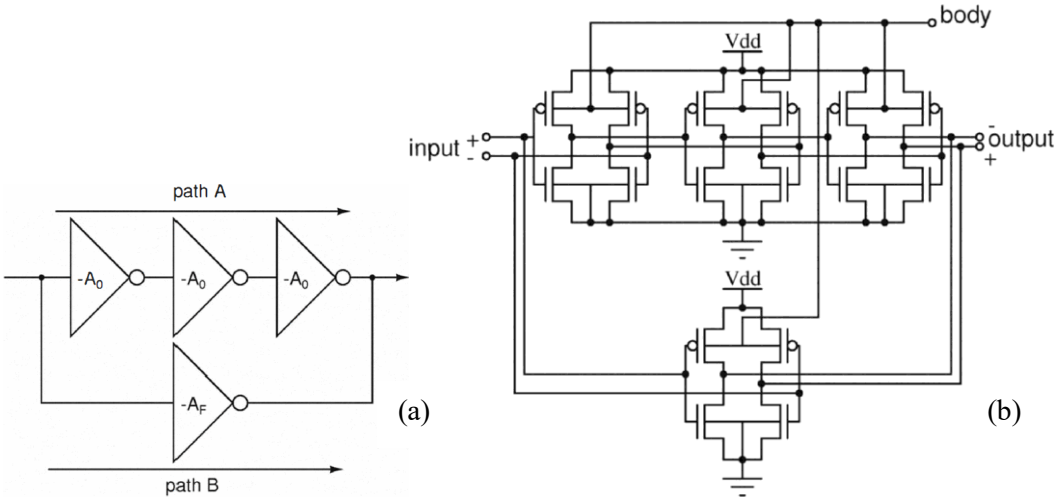

Figure 5 - (a) Block diagram for proposed opamp of [21]. (b) Transistor level implementation.

At low frequencies, the gain is dominated by the path A, $(A_0)^3$, with A_0 being the gain of each stage. In high frequencies, the path B, due to being faster, dominates the gain being only A_f, the gain of the feed-forward amplifier. The bandwidth product is given by A_f times the bandwidth of path B [21].

Besides the above mentioned feed-forward compensation technique, a biasing circuit is used to bias the n-well of the PMOS, Figure 6, with the purpose of increasing the individual gain of each stage around a common mode voltage of $V_{DD}/2$, irrespective of process, temperature, and supply voltage changes [21].

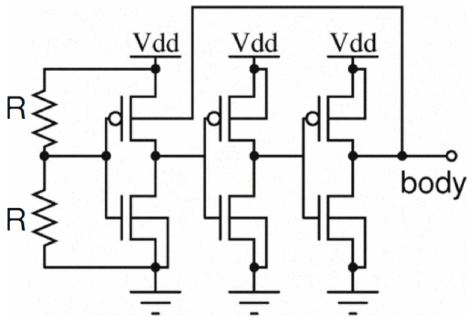

Figure 6 - Biasing circuit for the n-well [21].

The ratio of dimension between path A and B is chosen to allow the achievement of the desired phase margin. The cascaded stages of path A can be sized equally or can be sized with a progressive increase in order to achieve a larger phase margin, low power, and higher DC gain, for a given BW [21].

2.1.4 A 1.9 mW 250 MHz Bandwidth Continuous-Time ΣΔ Modulator for Ultra-Wideband Applications

A pseudo differential inverter-based OTA used in the loop filter is presented in [22] and shown in Figure 7.

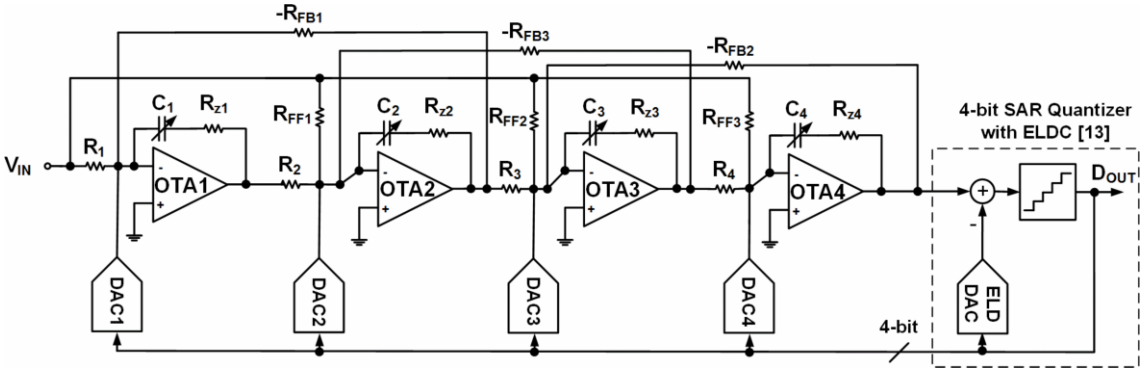

Figure 7 - Schematic of the single-ended continuous time ΣΔ modulator presented in [22].

In this application, the OTA 3 is implemented with a three-stage multi-path inverter-based, similar to the previous one. Meanwhile, OTA 1, 2, and 4 are implemented as single-stage inverter-based amplifiers. Using inverters for the analog amplifiers offers the benefits of supply current re-use and high bandwidth. Each OTA has a dedicated CMFB circuit, as shown in Figure 8, where it is presented the example of OTA 3 [22].

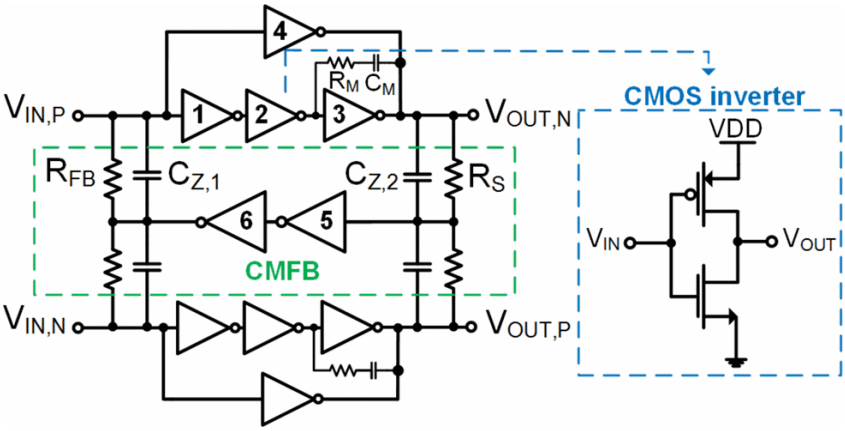

Figure 8 – Three stage pseudo differential inverter-based amplifier for OTA 3 [22].

The common mode is sensed by two resistors and amplified by two stage inverter-based common mode amplifier. The input common mode voltages are controlled by resistors R_{FB}. The CMFB loop is stabilized with the use of two capacitors [22].

2.2 Ring Amplifiers

The basic structure of the ring amplifier is presented in [13], Figure 9, further developed in [23], which serves as a starting point for the discussion of the structure and operation of the ring amplifier. A ring amplifier, or ringamp for short, is essentially a ring oscillator consisting of three inverter stages A1, A2, M_{CP}/M_{CN}. Without any modifications, this chain would start to oscillate when feedback is applied, Figure 10-(a). To avoid this and reach a state of stabilization, the ring amplifier is divided into two signal paths. The purpose of splitting a single path is to create a different voltage between nodes V_{BP} and V_{BN}, V_{BP} is lifted and V_{BN} is lowered, in order to create a range of input values for which neither output transistor M_{CN} nor M_{CP} of Figure 9 will fully conduct, resulting in the transient response presented in Figure 10-(b) [13].

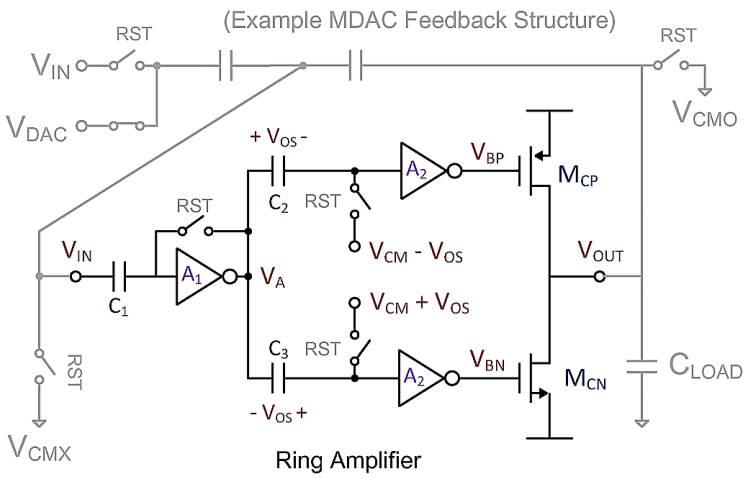

Figure 9 - The ring amplifier and basic switched-capacitor feedback primarily considered in the first half of paper [13].

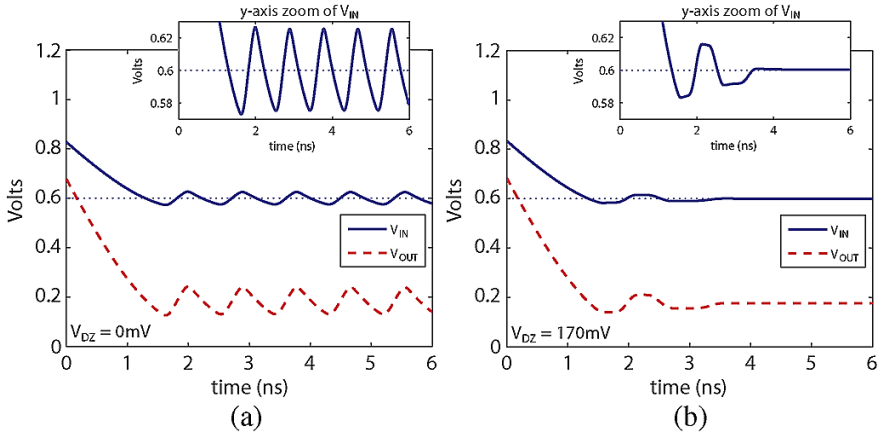

Figure 10 - Input and output charging waveforms when placed in the switched capacitor feedback structure (a)-without voltage deadzone (b)-with voltage deadzone [13].

If this non-conduction deadzone is sufficiently large, the ring amplifier will stabilize, dividing its operation into three regions: slewing, stabilization, and steady state, as represented in Figure 11.

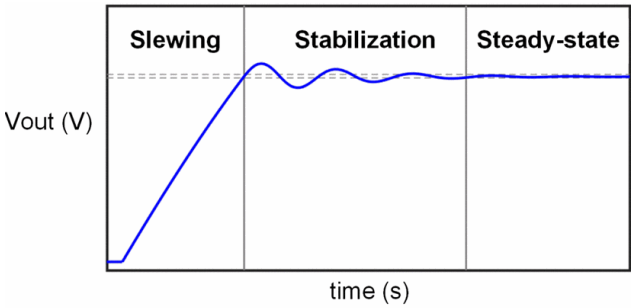

Figure 11 - Settling response of a ring amplifier [24].

The deadzone of the ringamp in Figure 9 is embedded prior to the second stage inverters by storing a voltage offset across capacitors C_2 and C_3. Any value for V_{IN} within the deadzone region is a viable steady-state solution for the ring amplifier, and the input-referred value of the deadzone will determine the overall accuracy of the amplifier for most practical cases [13].

In this basic structure, the deadzone voltage is placed between stages one and two. This is due to the fact that there are important stability benefits gained by embedding the offset prior to

the second stage inverters, rather than the first or third stage. It is typically desired to create an input-referred deadzone value of a few millivolts or less, and for medium accuracy ring amplifiers, embedding the deadzone offsets immediately after the first gain stage will create input-referred deadzone sizes small enough to achieve desired accuracies, while still keeping the embedded offset large enough to easily tune with a simple DAC or voltage reference. It is implemented using capacitors due to its capability to accurately and linearly set the deadzone offset value, while also allowing it to be done with a high-impedance, low-power reference [13].

Despite the simple structure of the ring amplifier presented in Figure 9, the theory behind it is not that simple. The approach usually used in opamp design is not the best one to analyze ring amplifiers with, because its behavior cannot be fully explained by considering each operational domain (DC, AC, transient) separately. This happens because the steady state, small signal, and transient characteristics of a ring amplifier are highly co-dependent [13].

One way to analyze a ring amplifier is to break the theory of operation down to several simple sub-concepts. As mentioned before, the ring amplifier operation can be divided into three phases of operation in time: slewing, stabilization, and steady state. Each phase can be broken down into a chain of cause-and-effect mechanisms [13].

2.2.1 Slewing

In this phase, the first two stages of the ringamp act like a pair of bi-directional continuous-time comparators that correctly select which output transistor (M_{CN} or M_{CP}) to use, depending on the value of the input signal, acting equivalently to the circuit of Figure 12 [13].

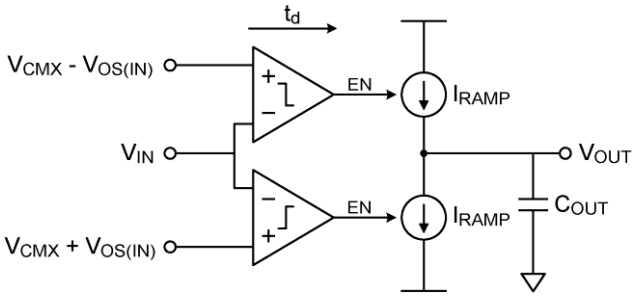

Figure 12 - Conceptual model of a ringamp during the initial slew-charging phase of operation in paper [13].

The selected output transistor charges the output load with a ramp, operating as a maximally biased current source. The ramping phase ends when the input signal crosses the threshold of the comparator and the current source turns off. Due to the finite time delay of the comparator, there will be some amount of overshoot beyond the comparator threshold [13].

2.2.2 Stabilization

After the initial charging ramp, the ringamp starts to oscillate around the target settled value with an amplitude ΔV_{init}, as can be seen in Figure 11. As mentioned before, with no deadzone, the structure continues to oscillate just like a three-inverter ring oscillator, Figure 10-(a) [13].

The ringamp reaches stabilization with the reduction of the peak overdrive voltage applied to the output transistors M_{CN} and M_{CP} on each successive period oscillation [13]. A different shifted replica of the oscillatory waveform generated at V_A is fed to each signal path. The upper path is given a replica where the peaks of the wave are lowered closer to the second stage inverter's threshold, and the lower path is given a replica where the troughs of the wave are raised closer to the threshold of the second stage inverter [13]. This results in a reduction in the frequency of the output pole of the ringamp, formed by the output impedance and C_{LOAD}. The reduction in output current due to V_{OV} reduction increases the output impedance (r_o) of the ringamp [13].

The relation between accuracy, speed, and power is explained in detail in [13]. For example, for a speed-oriented design, the initial ramp rate can be increased, or the time required to stabilize can be decreased. Both options mean that either accuracy (by increasing V_{DZ}) or power (by decreasing delay time) is sacrificed.

2.2.3 Steady-State

Based on the steady state operation of the third stage, ringamps can be divided into two classes. Class-B, where the third stage is completely off with a true deadzone, like the one described in [13] and class-AB-style, where the third stage operates at sub-threshold without a true deadzone but with a stability region [25].

2.3 Key Advantages

A. Output Compression Immunity

Any practical solution for scaled CMOS must use as much of the available voltage range as possible. As it turns out, ring amplifiers are almost entirely immune to output compression, and this enables them to amplify with rail-to-rail output swing [13].

B. Slew-Based Charging

The output devices M_{CN} and M_{CP} act like digitally switched current sources and charge the output with slew-based ramping. This is much more efficient when compared with a conventional opamp that charges the output load with some form of RC-based settling [13].

C. Performance Scaling with Process

A ring amplifier, for its similarities with a ring oscillator, is a prime candidate to benefit from the process scaling. For this to be true, it must meet two criteria. The first one is that the technique must operate efficiently in a scaled environment, and the second one is that the technique must inherently scale with advancing process technology, improving in performance simply by migrating into a newer technology [13].

2.4 Improved Topologies of Ring Amplifiers

With the key principles and the basic structure described in [13] in mind, different structures for ring amplifiers emerged, each one with its purpose.

2.4.1 Self-Biased Ring Amplifier

The amplifier proposed in [25], Figure 13, differs from the one in [13] in the way that it creates the deadzone voltage. The external biases, switches, and capacitors are eliminated, reducing the loading of the first stage, allowing it to reduce the power consumption, and the deadzone voltage is created by a resistor, R_B, between the drains of the second stage inverter. Due to the inverter short circuit current, R_B dynamically applies an offset to the gate voltages V_{CP} and V_{CN} of the third stage inverter [25].

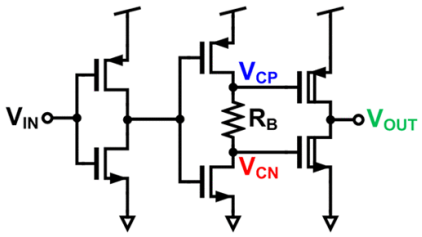

Figure 13 – Schematic of ring amplifier with dynamically applied offset using a resistor R_B in the second stage inverter presented in [25].

Another difference is the introduction of high threshold devices in the third stage. These devices present orders of magnitude higher output resistance, extending the V_{OS} range and therefore increasing the PVT robustness. However, these devices also reduce the slewing current of the ring amplifier [25].

A noise reduction solution is also present in [25]. The solution presented is the reduction of the first stage power supply using a diode-connected NMOS, M_{NR}, Figure 14. This allows the reduction of thermal noise without increasing power consumption.

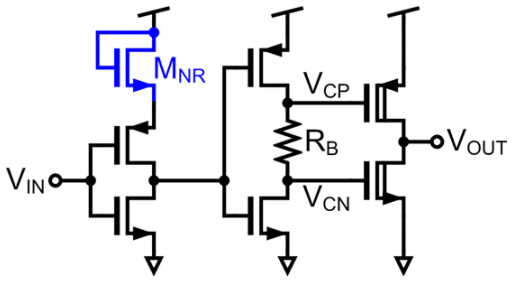

Figure 14 – Example of a self-biased ring amplifier presented in paper [25], where M_{NR} is used as an internal power-regulator of the first inverter.

2.4.2 Current-Starved Inverter Ring Amplifier

The strategy for creating the deadzone voltage in [26] is to use current-starved inverters in the second stage, Figure 15. The devices M_{2CP} and M_{2CN} operate as triode resistors changing the trigger point of the inverters. The deadzone is controlled by the voltages V_{ctrln} and V_{ctrlp}.

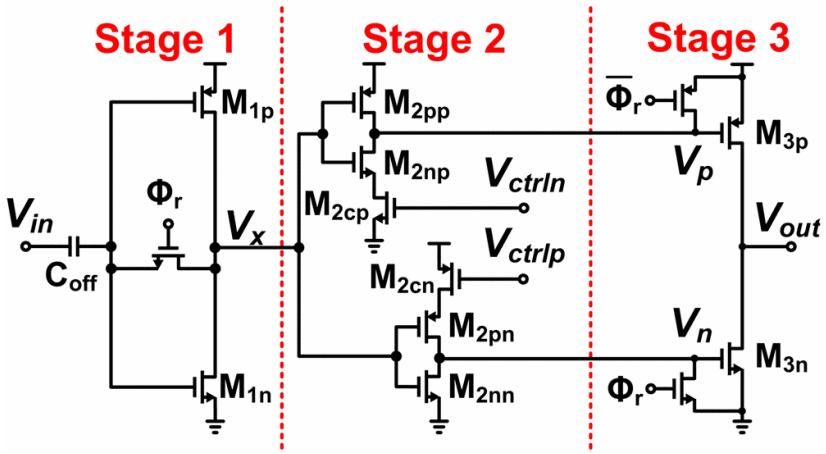

Figure 15 - Single-ended topology of a pseudo differential current-starved inverter ringamp as designed in [26].

2.4.3 Ring Amplifier using Deadzone Regulation Circuit

Due to the high susceptibility to process variations of ring amplifiers, in [24] is presented a way to complement the previous topology and make the ringamp more robust to process variation.

The gate bias voltages V_{GPREF} and V_{GNREF} are set by the diode-connected transistors and the constant current source, observable in Figure 16. These voltages track the threshold voltage variation across process corners for a fixed bias current [24].

A negative feedback loop is formed using the replica of the second stage inverters and the error amplifiers. Each error amplifier senses the steady state output of the replica of the second stage and sets the control voltages V_{CTRLN} and V_{CTRLP}, in a way that the steady state value of the second stage output approaches the reference bias voltages V_{GPREF} and V_{GNREF}, respectively. This negative feedback action regulates the quiescent current I_Q in the third stage inverter [24].

By appropriately choosing the value of I_{BIAS} as a factor of the required I_Q, the control voltages V_{CTRLN} and V_{CTRLP} obtained from this circuit, can be used in the ring amplifier shown in the previous section, Figure 15, for process invariant operation [24].

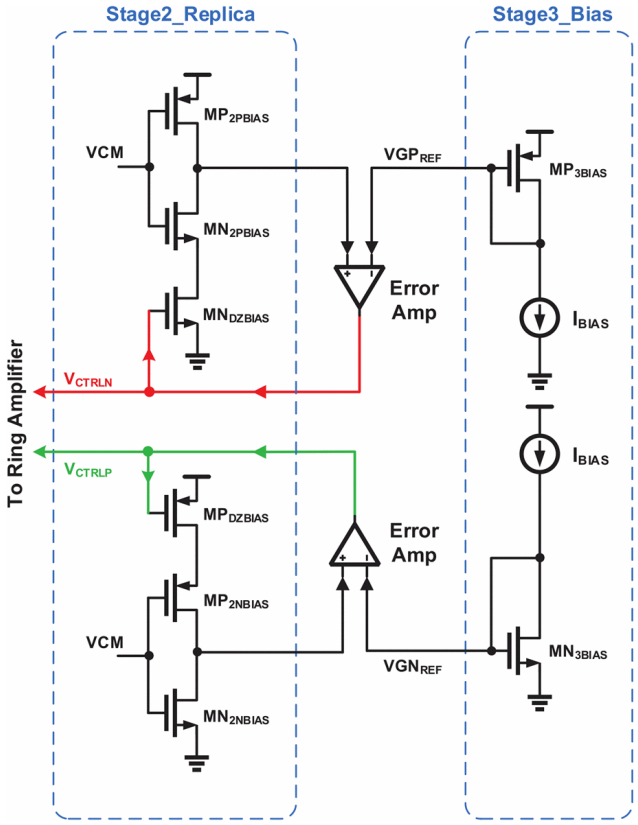

Figure 16 - Deadzone regulation circuit for current starved inverter based ring amplifier proposed in [24].

2.4.4 Ring Amplifier with CMOS Resistor

The ringamp presented in Figure 17 is based on the self-biased implementation presented in [25], as mentioned in section 2.4.1. However, instead of using a poly-silicon resistor, an anti-parallel (AP) arrangement of CMOS transistors is used, providing the capabilities of both powering down the amplifier and tunning the deadzone voltage [27].

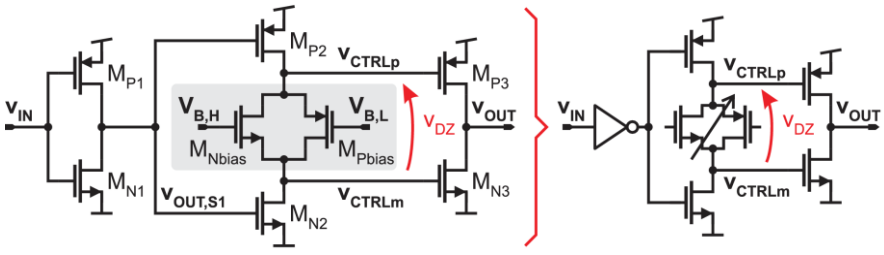

Figure 17 - Core schematic along with the simplified representation of the Ring Amplifier with CMOS Resistor from paper [27].

Depending on which phase of operation the ringamp is in, the AP CMOS arrangement changes its behavior. During the slewing phase, it behaves like a CMOS resistor, the second stage devices M_{P2} and M_{N2} operate (mutually exclusively) in triode and cutoff regions, pulling V_{CTRLp} and V_{CTRLm} towards one of the supplies. The voltage difference at the nodes of the AP CMOS arrangement becomes smaller than $V_{DS,sat}$ of M_{Pbias} and M_{Nbias}, so these devices operate in the triode region, whose resistance decreases as V_{CTRLp} and V_{CTRLm} are pulled towards the target supply rail [27]. During both stabilization and settling, the DZ voltage builds up, the voltage

difference at the nodes of the AP CMOS arrangement increases past the $V_{DS,sat}$ of $M_{Pbias,}$ and $M_{Nbias,}$ pushing these devices into saturation. It behaves like the floating battery used in the Monticelli class-AB output stage [27].

For the power down of the amplifier, the AP CMOS arrangement can easily be put into a high-impedance state by pulling $V_{B,H,}$ and $V_{B,L}$ to the supply rails [27].

The magnitude of the deadzone voltage, studied in [27], has a critical role in the determination of the ringamp transient behavior and is especially important in high-speed applications where the ringamp is made to operate on the verge of incomplete settling. With a small VDZ, the overdrive of the output stage is the largest and is reached with minimum delay, causing a fast slewing of the output. However, this DZ voltage is too small to enforce settling. With a higher VDZ, the overdrive of the output stage is the smallest and is reached after a larger delay, resulting in the slowest slewing of the output voltage. So, to achieve the desired behavior, proper sizing is required to achieve a deadzone voltage that presents the best trade-off between delay time and speed of slewing for the application.

2.4.5 Fully Differential Ring Amplifier

Most ring amplifiers have single-ended topologies, therefore have all the disadvantages of single-ended structures. Some of these disadvantages can be alleviated by pseudo differential common mode feedback, as discussed in [13], [25], shown in Figure 18.

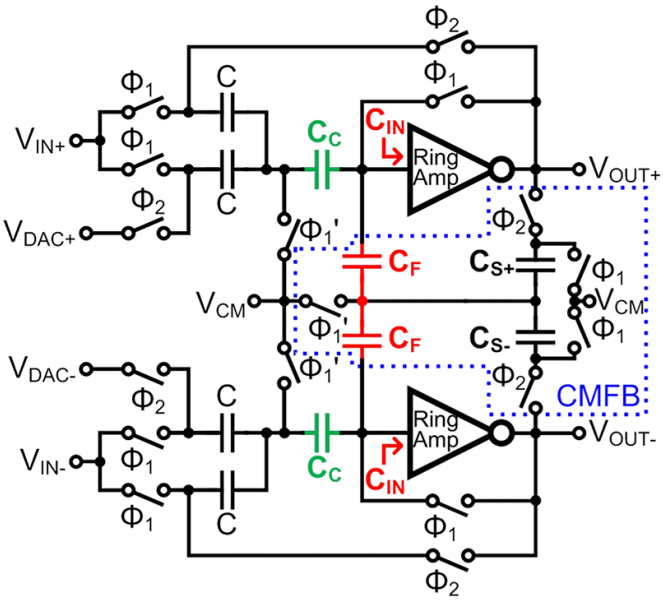

Figure 18 – Pseudo Differential MDAC gain stage as used in [28].

A fully differential topology based on the self-biased ring amplifier of [25] is proposed in [28], shown in Figure 19. A differential pair was used in the first stage. The first stage functions as a current starved inverter for the common mode of the input, because it has both PMOS and NMOS tail current sources. The first stage also uses a current re-use technique to reduce thermal noise. The second and third stages are inverter-like structures, with the second stage using high V_{Th} devices to prevent gain reduction and the third stage using high V_{Th} devices to extend the second stage output voltage range for which the transistors operate in saturation [28].

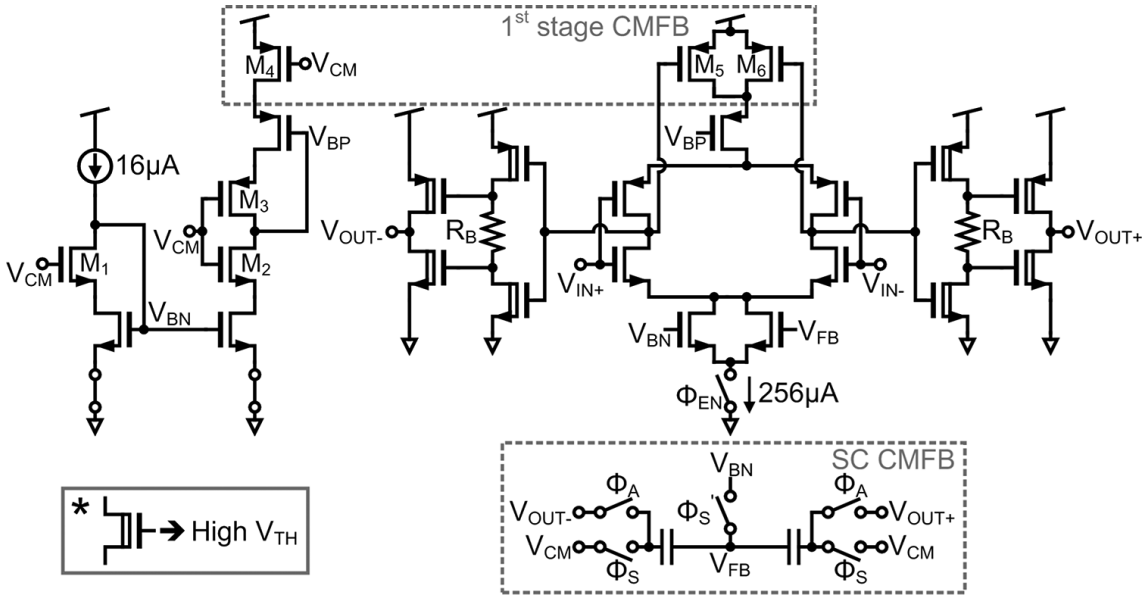

Figure 19 – Schematic of [28] - Fully differential ring amplifier, biasing circuit, and CMFB.

3. Proposed Ring Amplifier Topology

The main purpose, based on the concepts presented in the previous sections, is to achieve a ring amplifier that has a simple structure and simple sizing, but fast and PVT robust that suits the industrial needs.

As previously explained in section 2.4.5, the best approach is a fully differential topology. This allows for a better common mode and supply rejection. However, to extend the bandwidth of the first stage to a higher frequency, a non-cascode stage with less parasitic capacitance has to be used.

To create the deadzone voltage, the strategy described in section 2.4.4 is adopted since it is a more simple structure and allowing an easier method to adjust this voltage. As described in [27], an important part of the transient behavior is dependent on the deadzone voltage. Since these structures are very sensitive to PVT variations, a biasing structure is used in the gates of the transistors of the CMOS resistor similar to the one presented in [24]. This biasing circuit sets the desired voltage in the third stage replica by a current source and a diode-connected transistor and it compares that voltage with the one in the second stage replica using an error amplifier. If those voltages are different, the error amplifier applies a different voltage, proportional to the difference, to the gate of the bottom device. An ideal error amplifier is used due to it not being the focus of this study, and due to it being an easy block to implement, only needing to be a 30 dB gain amplifier like a differential pair.

Due to the load differences between the two phases, ring amplifiers tend to have different settling in each phase. To mitigate this, a switch is added in the first stage, as used in [29]. This solution allows for a very quick stabilization in the reset phase, due to the elimination of the pole of the first stage. Another option that addresses this problem is the one described in [25] where they add a different load in the reset phase. However, this proved to be less effective and used up more area.

The proposed topology for the ring amplifier studied in this thesis is presented in Figure 20 and in Figure 21 is presented its biasing circuit.

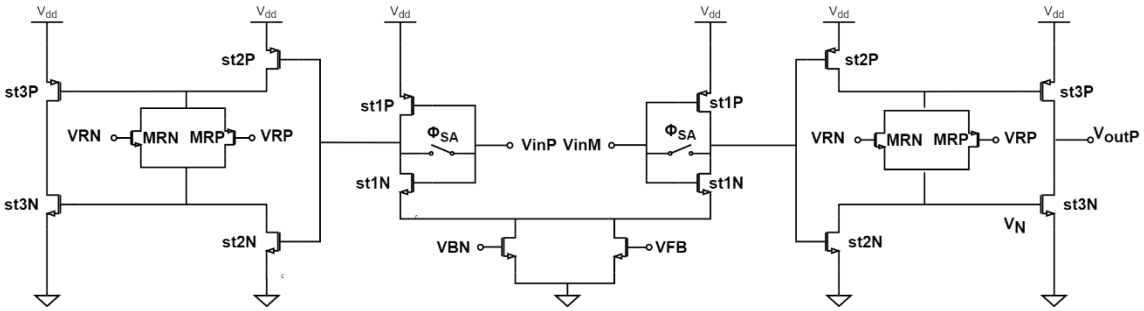

Figure 20 - Schematic of the proposed Fully Differential Ring Amplifier.

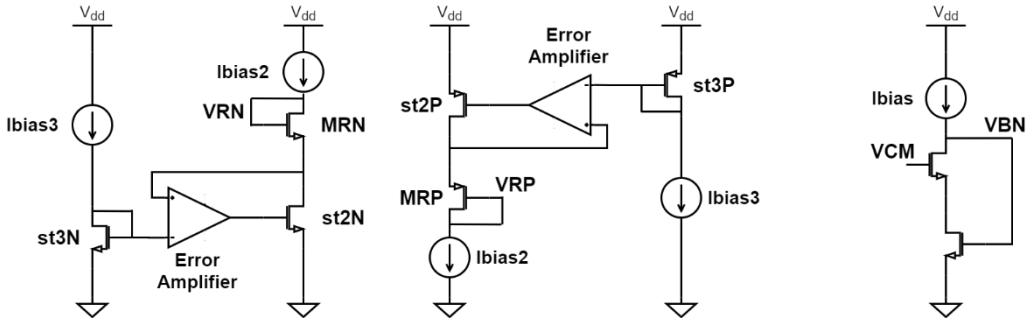

Figure 21 – Schematic of the proposed Biasing Circuit for driving the CMOS Resistor and for the Differential Pair.

4. Design Methodology

Both structure and operation of a ring amplifier are quite different from a conventional amplifier, as it was explained in section 2.2. Therefore, the usual design approach used for conventional amplifiers cannot be used in ring amplifiers. The best way to reach an optimum sizing for this kind of amplifier is by iterations. However, to avoid the usage of complicated optimization processes like in [30] and to have a simple and intuitive sizing system, one way to address the problem is to find the optimum sizing of each stage for a given gain, speed, stability, and noise [31].

A. Gain

Due to it being a three-stage topology, the ringamp can achieve high gain values. This happens because, at the steady state, all three stages contribute to the gain. Hence the gain expression yields:

$$A_v = (g_{mN} + g_{mP})(r_{oN} \parallel r_{oP}) \tag{1}$$

where g_{mN}, g_{mP}, r_{oN}, and r_{oP} correspond, respectively, to the transconductance and output resistance of the NMOS and PMOS transistors.

It is here that we are presented with the first trade-off. As can be seen in Equation (1), the small-signal gain is a function of the channel length (L) of the transistor. To obtain a higher gain, the L has to be increased, however, this translates to a reduction in the bandwidth, as the parasitic capacitors are increased. Therefore, the ideal scenario is to choose the smallest L that fulfills the required gain, to maximize the BW [31].

B. Speed

The speed of the amplifier is defined by the settling time and stabilization time. To design a ringamp that is as fast as possible, the ideal scenario is to have no oscillation phase. This time will depend on the BW settling of the ringamp [31].

As explained in 2.2, the first and second stages select which third stage device charges the load capacitance, C_L. The slew rate, given by Equation (2), where I_{RAMP} is the current provided by the third stage at the initial slewing phase and V_{Th} is the threshold voltage of the transistor, is directly proportional to (W/L) of the third stage inverter [31].

$$SR = \frac{I_{RAMP}}{C_L} = \frac{\frac{1}{2}\mu C_{ox}\frac{W}{L}_3\left(V_{GS,3} - V_{Th}\right)^2}{C_L} \tag{2}$$

Due to T_{delay}, this phase ends with an overshoot voltage given by:

$$V_{overshoot} = \frac{I_{RAMP} \cdot T_{delay}}{C_L} \tag{3}$$

This overshoot voltage needs to be reduced to guarantee proper operation. Having a positive phase margin is a necessary condition, however, this condition alone does not guarantee a proper operation, due to the changing of the dynamic current during its operation, described in 2.2. This represents again a trade-off between the sizing of the second and the third stages to achieve a compromise between the slew rate and the delay time, to achieve the best settling time, choosing the (W/L) for the third stage that satisfies a good slew rate with the whole required settling time. The size chosen for the third stage sets a certain load capacitance on the first stages. The second stage size is chosen to achieve the minimum delay for the first two stages [31].

C. Stability Considerations

To stabilize the ring amplifier, a dominant pole is created through biasing the third stage in a sub-threshold, which leads to increasing the output resistance to form a dominant pole with C_L. With the increase of the offset voltage, the output stage is biased more into sub-threshold, which leads to a better phase margin at the expense of lowering the entire ring amplifier bandwidth [31].

The overall transfer function in the stabilization phase is presented in Equation (4), with each stage inverter contributing with one pole (P), $P_1 = \frac{1}{r_{o1}C_{p1}}, P_2 = \frac{1}{r_{o2}C_{p2}}, P_3 = \frac{1}{r_{o3}C_{p3}}$, and $C_{p3} \cong C_L$ [31].

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}r_{o1} \cdot g_{m2}r_{o2} \cdot g_{m3}r_{o3}}{(1 + s/P_1)(1 + s/P_2)(1 + s/P_3)} \tag{4}$$

D. Noise Analysis

The thermal noise dominates the noise performance. The first stage inverter is the dominant source of noise [31].

The thermal noise of an inverter is given by:

$$\overline{V_{n,in}^2} = \frac{4KT\gamma}{g_{mN1} + g_{mP1}} \tag{5}$$

where K is the Boltzmann constant, T the temperature in Kelvin, and γ is a process dependent parameter. As it can be seen in Equation (5), to reduce the input-referred noise, the transconductance must be increased, resulting in the first stage being the most power-hungry stage of the ring amplifier [31].

E. Design Procedure

The design strategy combines the circuit specifications with the trade-offs above mentioned, resulting in the diagram presented in Figure 22. To summarize, the amplifier noise is mostly dominated by the first stage inverter, the second stage is responsible for the stability and phase delay, and the third stage sets the slew rate [31].

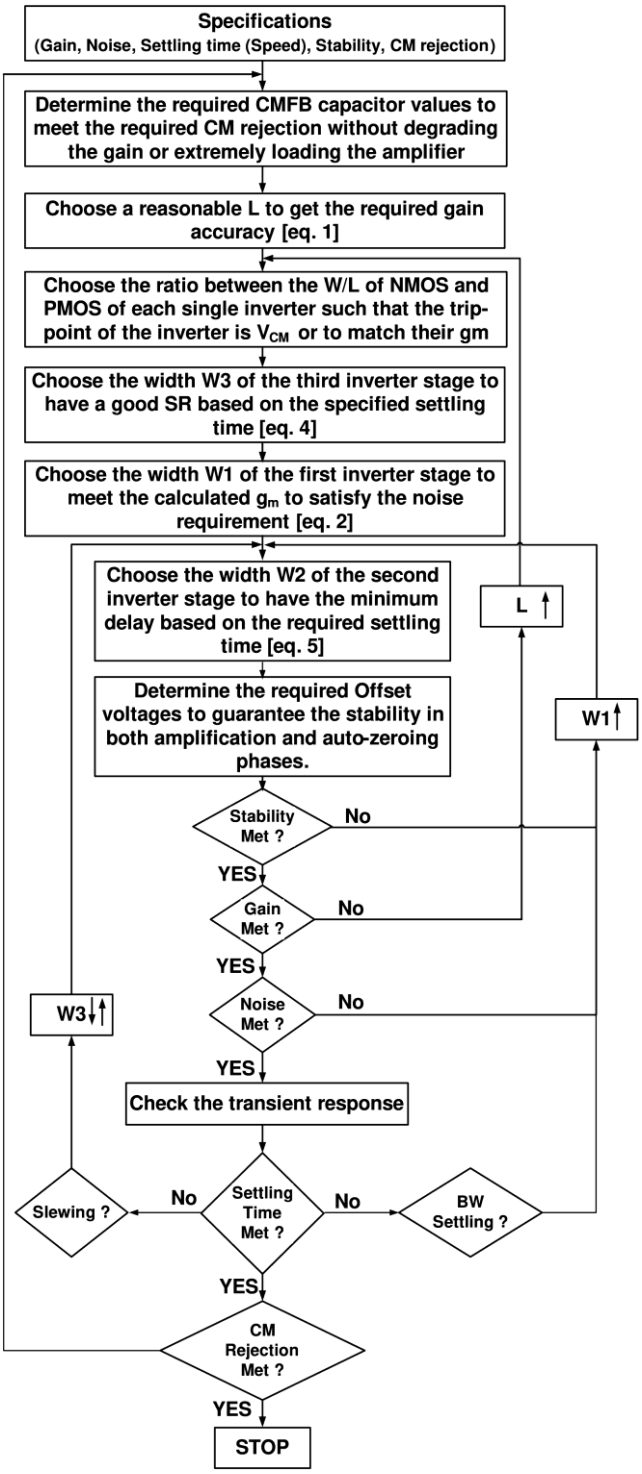

Figure 22 – Diagram of the proposed systematic design and sizing methodology [31].

4.1 Technology Limitations

The target technology is 7 nm FinFET CMOS from TSMC with XILINX parameterized cells. In these parameterized cells, not all sizes are available, as is possible to see in Figure 23, the value for *W* is fixed at 98 nm and exists three values for *L*, 8 nm, 11 nm, and 36 nm. The size of the devices is changed by changing the multiplier number.

Figure 23 - Transistor parameterized cell.

5. Simulation Testbench

All designs and simulations have been performed using the software from Cadence Design Systems. The schematics for each structure were created using the Virtuoso System Design Platform, while the simulations for each respective circuit have been carried out in the Spectre Circuit Simulator.

The testbench used to simulate the ring amplifier and the common mode feedback circuit are presented in Figure 24 and Figure 25, respectively. In Appendix A is presented the schematics from Cadence Virtuoso, Figure 52, Figure 53, and Figure 54.

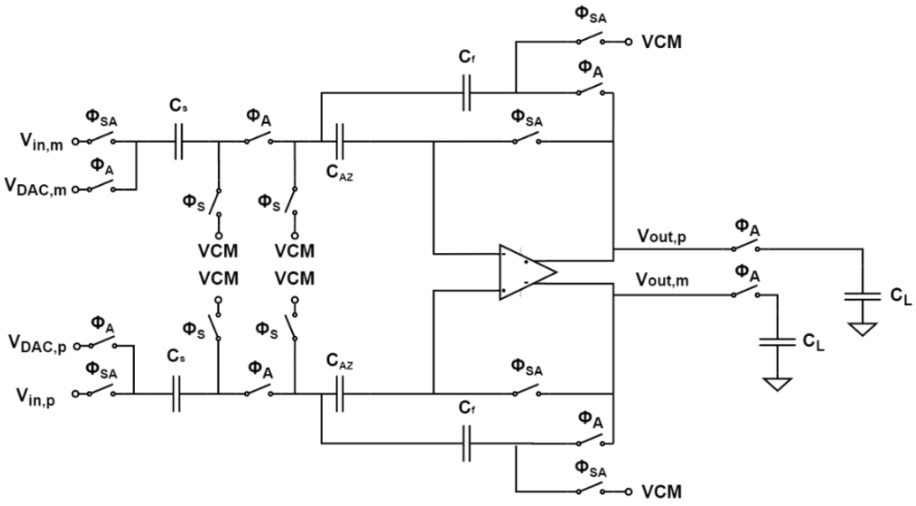

Figure 24 - Testbench for the fully differential topology.

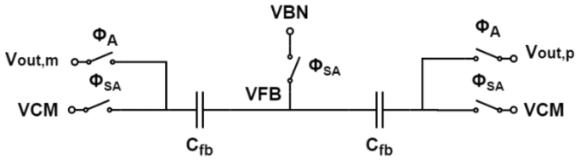

Figure 25 - Common mode feedback circuit.

The clock signals controlling the switched capacitor network are divided into three phases: the amplifying phase in red, the sampling phase in pink, and an advanced sampling phase in yellow. This advanced sampling phase exists to guarantee the correct transfer of charges between the capacitors. The mentioned phases are non-overlapping as can be seen in Figure 26. A larger representation of the clock signals is represented in Appendix A, Figure 55.

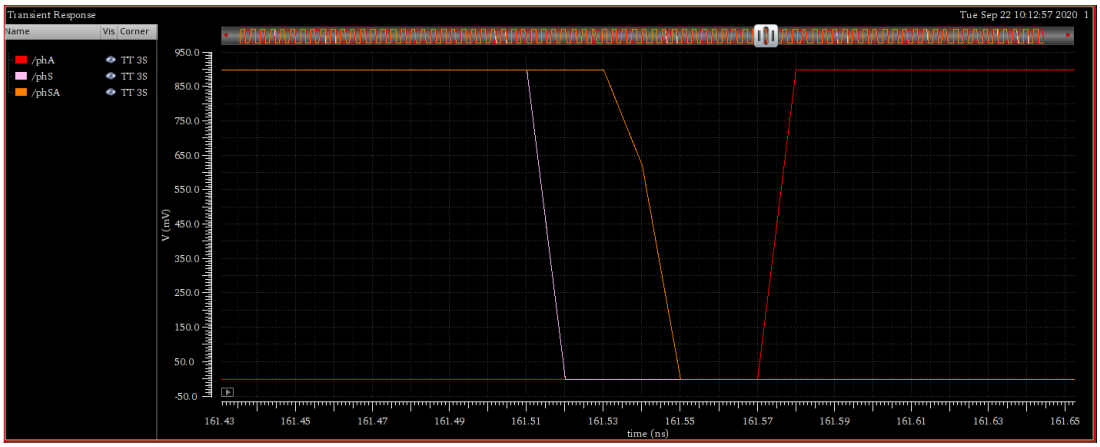

Figure 26 – Close-in of phase transition in clock signals.

The table below, Table 1, shows the values for the capacitors and voltages sources. Similar to the parameterized cells of the transistors, also the MOM caps have Xilinx parameterized cells from TSMC 7 nm technology node, in this case, with an equal number of horizontal and vertical fingers, 15, resulting in a capacitance of 25.27 fF. To reach the desired capacitance, the multiplier number is increased. The table presents all the variables used for the FFT simulation as well, guaranteeing a coherent sample.

Table 1 - Global Variables for FD Testbench.

Variable	**Cf**	**Cs**	**C_{LOAD}**	**C_{AZ}**	**V_{DD}**	**V_{dac} V_{CM}**	**$V_{in,ac}$**	**$V_{in,amp}$**	**$V_{in.dc}$**
Value	12	24	28	36	900 mV	$\frac{V_{DD}}{2}$	1 V	25 mV	450 mV
	303.24 fF	606.48 fF	707.56 fF	909.72 fF					
Variable	**Cycle Number**	**F_{sample}**	**Prime Number**	**Sample Points**		**Num Points**		**Phase Margin**	
Value	15	100 MHz	11	256		32		20 ps	
Variable	**Bin**		**$V_{in,freq}$**		**Stoptime**		**Phase Period**		
Value	$\frac{F_{sample}}{Sample\ Points}$		$Bin \times Prime\ Number$		$\frac{Cycle\ Number}{V_{in,freq}}$		$\frac{1/V_{in,freq}}{Num\ Points} \times 4$		

The primary objective of this study is to analyze the functionality in 7 nm technology node. The first thing to guarantee is a proper transient response as described in previous chapters. After that, an AC analysis can be performed with the particularity of doing it at three different times, each one in each operation phase of the ringamp, slewing, stabilization, and steady state. This is important because it helps, in an initial phase, to understand the operation and pole movement towards stabilization. In Table 2 is presented the selected times for the AC analysis.

Table 2 – Selected times for AC analysis.

Slewing Phase	1.56505 µs
Stabilization Phase	1.56522 µs
Steady State	1.56725 µs

Another important simulation is the FFT, extracting the values for SNR, SFDR, THDDB, and ENOB equivalent, both with and without transient noise. For the analysis with transient noise was considered the worst-case noise.

All the mentioned analyses are performed over corners. Over corners analysis refers to simulations with PVT variations, process, supply voltage, and temperature. Regarding the supply voltage variation, it was concluded in early stages that it would not be a problem with the structures used in this thesis, so the simulation foci were the process and temperature variations. The process variations were SS; FF; SF and FS. Each one with two temperatures, -40°C and 125°C. Besides that, the typical process corner was also simulated with a temperature of 85°C.

6. Simulation Results and Discussion

The results for three different structures will be presented and compared in this chapter: the one presented in section 2.4.4 and a fully-differential variation of the one in section 2.4.3 (as they were both the more promising structures), and the proposed topology presented in chapter 3.

The analysis of the results will prioritize the transient response. When the structure presents a satisfactory behavior over time, the rest of the results are analyzed. Due to the focus being the functionality of the ring amplifier in this technology node, there are no strict specifications to fulfill, but there are target values for settling time and gain, described in Table 3.

Table 3 – Target specifications.

Specification	Settling Time	Gain
Value	100-200 ps	>60 dB

6.1 CMOS Resistor Pseudo Differential Ring Amplifier

Most ring amplifiers presented in literature are single ended with pseudo differential feedback topologies, so it is interesting to compare the results of that kind of ring amplifier to results from fully differential ringamps.

To simulate the pseudo differential topology is used the topology presented in Figure 18. The schematic from Cadence Virtuoso is presented in Appendix B, Figure 56. The ringamp schematic, presented in Appendix B, Figure 57, is similar to the one presented in section 2.4.4, Figure 17.

The values for the capacitors and the variables needed in the testbench, similar to Table 1, are shown in Table 4. In Table 5 is presented the multiplier value for each device of the schematic of Figure 57. Both transistors in each stage have the same size, therefore stage 1 is referring to both PMOS and NMOS from the first stage, and the same goes for the next two stages. MRP and MRN are referring to the transistor composing the CMOS resistor, MRPbias and MRNbias compose the biasing circuit with Ibias.

Table 4 - Global Variables for PD Testbench.

Variable	**C**	**Cc** **C_{LOAD}**	**Cf** **Cs**	**V_{DAC}**	**V_{DD}**	**V_{CM}**	**$V_{in,ac}$**	**$V_{in,amp}$**	**$V_{in.dc}$**
Value	12 303.24 fF	25 631.75 fF	10 252.70 fF	450 mV	900 mV	$\frac{V_{DD}}{2}$	1 V	100 mV	450 mV
Variable	**Cycle Number**	**F_{sample}**	**Prime Number**	**Sample Points**		**Num Points**		**Phase Margin**	
Value	10	100 MHz	13	32		32		20 ps	
Variable	**Bin**		**$V_{in,freq}$**		**Stoptime**		**Phase Period**		
Value	$\frac{F_{sample}}{Sample\ Points}$		$Bin \times Prime\ Number$		$\frac{Cycle\ Number}{V_{in,freq}}$		$\frac{1/V_{in,freq}}{Num\ Points} \times 4$		

Table 5 - Device Sizing for CMOS Resistor PD.

Global Variable	Stage 1	Stage 2	Stage 3	MRP MRN	MRPbias MRNbias	Ibias
Value	65	15	1	1	40	250 µA

The transient response over corners of the pseudo differential topology is presented in Figure 27. It is possible to observe that, besides showing a slow response, the main problem is the huge variation over corners. This variation may be originated from the fact that the structure is pseudo differential, therefore not having an inherent common mode. The pseudo differential common mode feedback structure helps to alleviate this disadvantage, however, the results prove that it isn't enough. This is the main reason for pointing the research towards fully differential topologies that do not present this kind of problem.

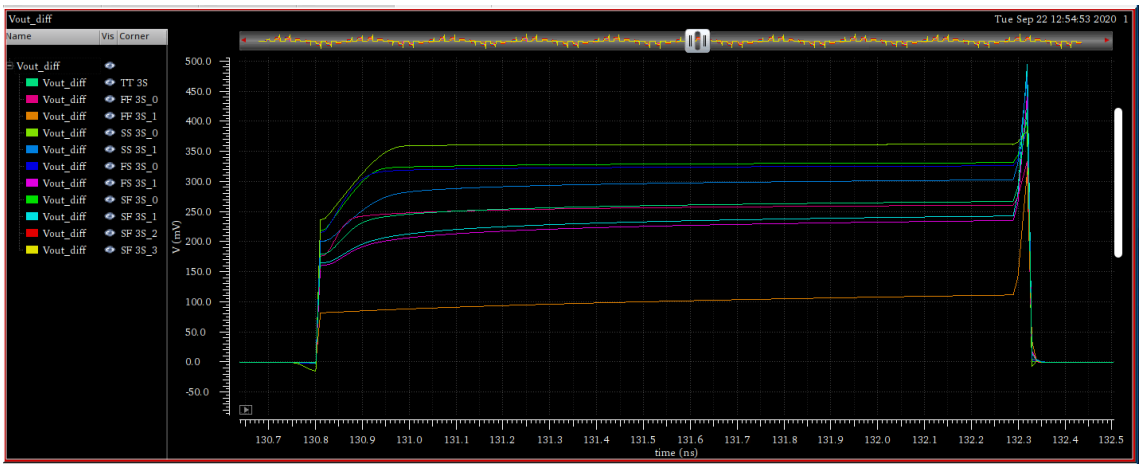

Figure 27 - Transient response over corners for CMOS Resistor topology PD.

6.2 Current Starved Fully Differential Ring Amplifier

With the purpose of obtaining less corner variation, a fully differential version of the ring amplifier with the deadzone regulation circuit presented in section 2.4.2 is tested using the testbench presented in chapter 5, with the Cadence Virtuoso schematic presented in Appendix C, Figure 58 for the ringamp, and Figure 59 for the biasing circuit. In this case, the error amplifier is represented by ideal elements such as an ideal voltage-controlled current source, resistor, and capacitor. This is done because it is an easy block to implement and it is not a fundamental block of the research.

The values for the multiplier number of each device of the schematic, the current sources, and the elements of the error amplifier are presented in

Table 6. These values were obtained by the methodology presented in section 4, Figure 22, through several iterations to guarantee the desired behavior. Similar to the previous section, stage 1 is referring to both devices in the first stage since both present the same size, and so on for each stage. Stage 2 tail refers to the current starved devices in the second stage, being both PMOS and NMOS equal in size. Gain error refers to the error amplifier gain, Gm error to the transconductance, and C error emulates the parasitic capacitance of the error amplifier. MBN and MFB represent the bottom devices of the first stage. *Ibias3* and *Ibias* V_{BN} define the current in each biasing circuit.

Table 6 - Device Sizing for CS FD.

Global Variable	Stage 1	Stage 2	Stage 2 Tail	Stage 3	MBN MFB	C error	Gain error	Gm error	Ibias3	Ibias V_{BN}
Value	75	15	20	2	80	10 fF	30	10 mS	250 µA	500 µA

The transient response over corners of the current starved ringamp is shown in Figure 28. When compared with the transient response presented in Figure 27 it is clear that the fully differential topology presents much less variation over corners. Although, it is not a completely

fair comparison, because one is based on the self-biased ring amplifier concept and the other creates the deadzone voltage by a current starved second stage.

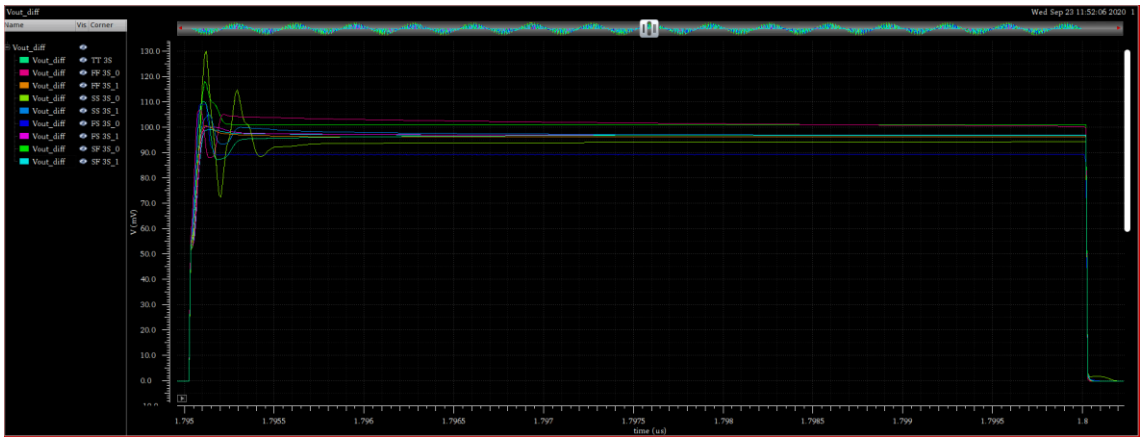

Figure 28 - Transient response over corners for the FD Current Starved.

In the next figure, Figure 29, is shown how the settling time was measured. The corner shown is the typical. In Table 7 is presented the settling time values for all corners.

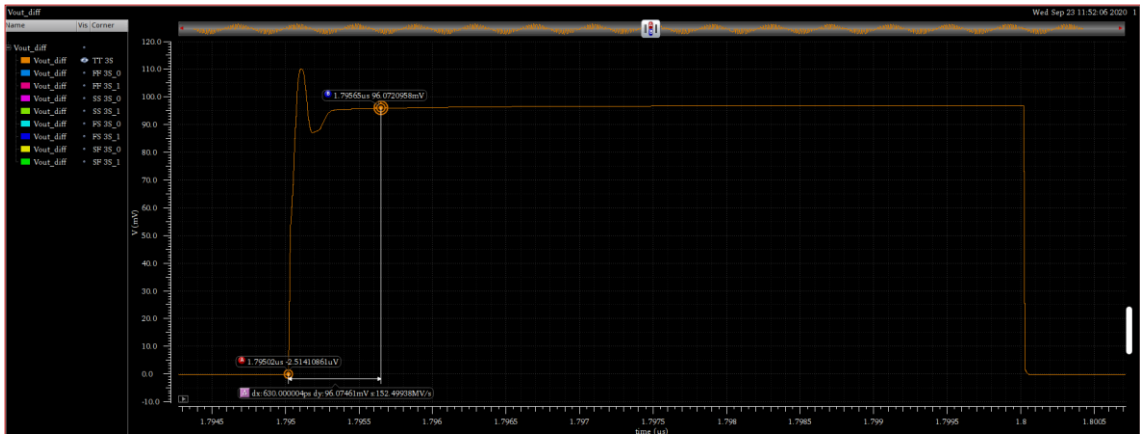

Figure 29 - Settling time measure for the typical corner of the current starved ring amplifier.

The select times, from Table 2, for the AC analyses are represented in Figure 30. Each time corresponds to a different phase of operation as already mentioned. The three times are represented in the differential output of the ringamp in the typical corner.

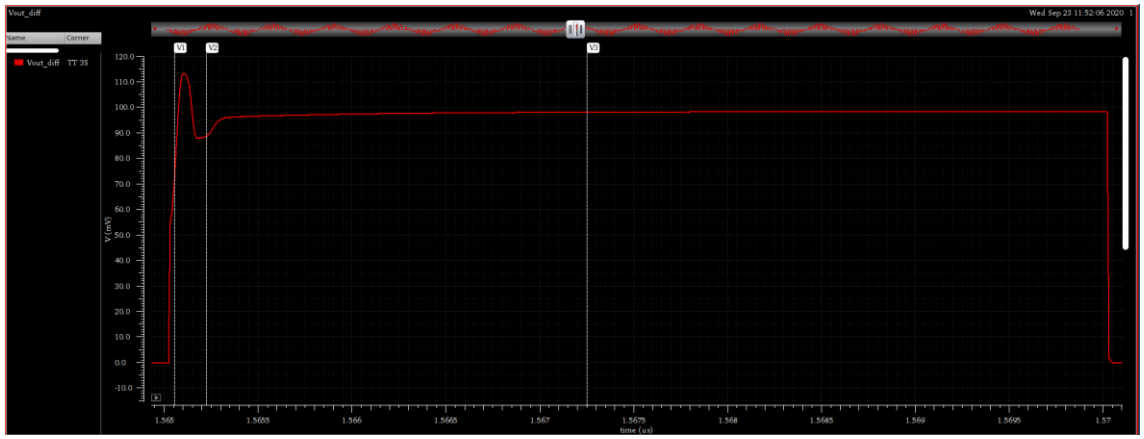

Figure 30 - The three selected times for the AC analysis in the three different phases of the current starved ring amplifier: slewing, stabilization and steady state.

The AC response of the current-starved ring amplifier is presented from Figure 31 to Figure 34. Figure 31 and Figure 32 show the gain and phase response, respectively, of the typical corner, where it is possible to see clearly the pole movement toward stabilization, characteristic of the operation of these kinds of amplifiers. In Figure 33 is represented the gain over corners on the steady state. It is possible to observe that all corners present a high gain however the bandwidth presents a huge variation.

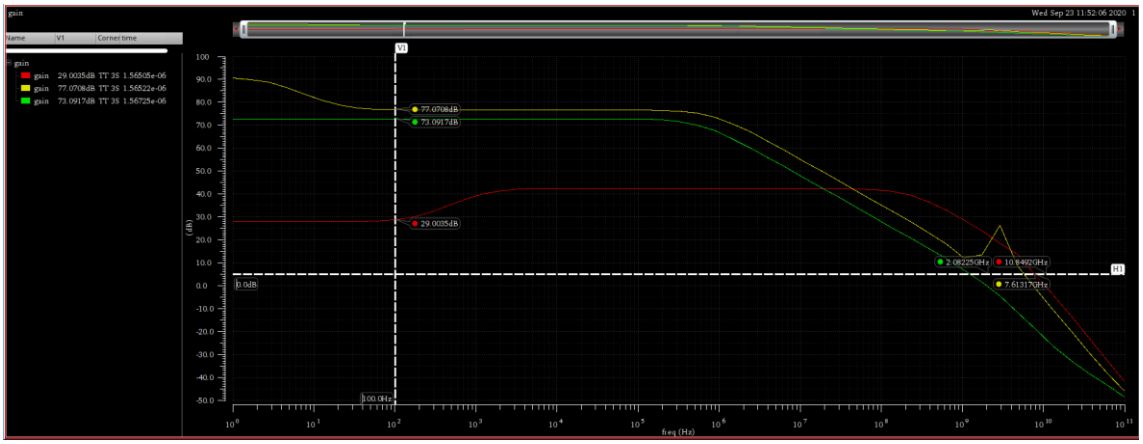

Figure 31 - Gain for each phase of operation of the current starved ring amplifier. Red for slewing phase, yellow for stabilization phase and green for steady state.

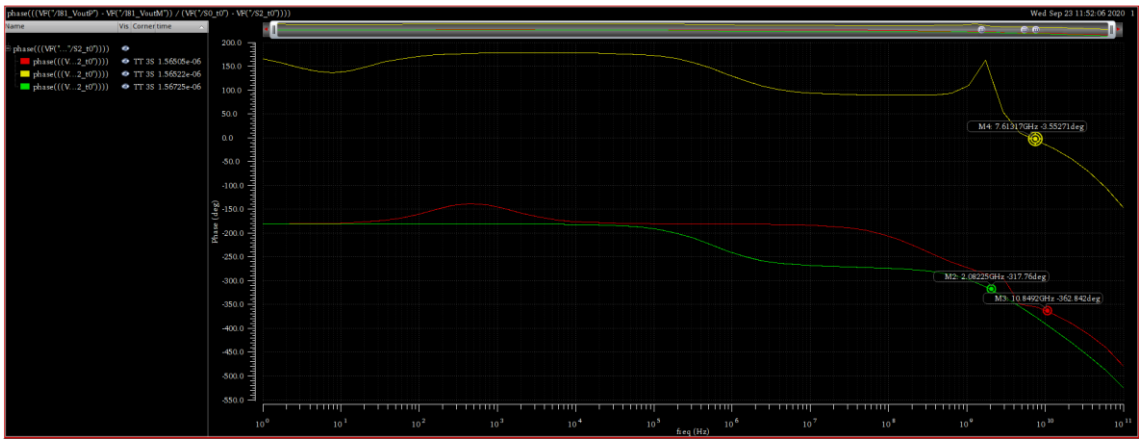

Figure 32 - Phase for each phase of operation of the current starved ring amplifier. Red for slewing phase, yellow for stabilization phase and green for steady state.

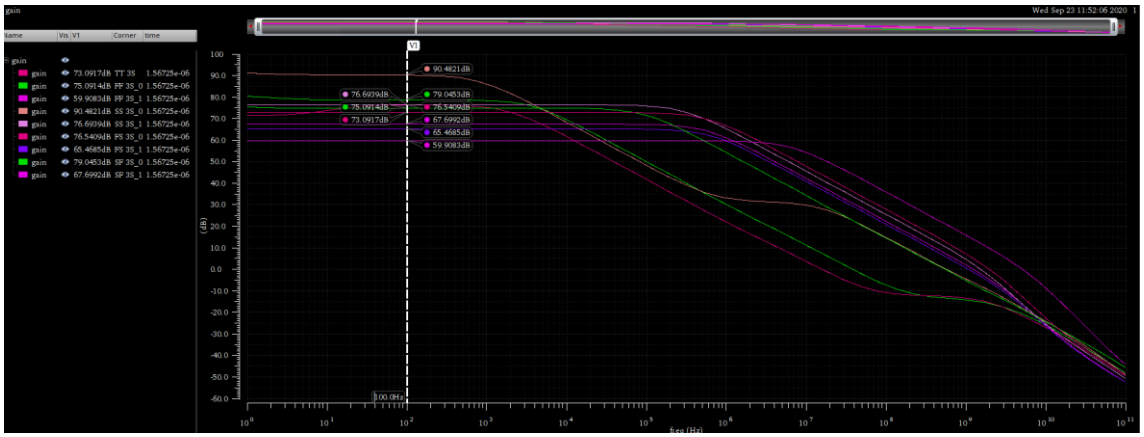

Figure 33 - Gain over corners of the steady state of the current starved ring amplifier.

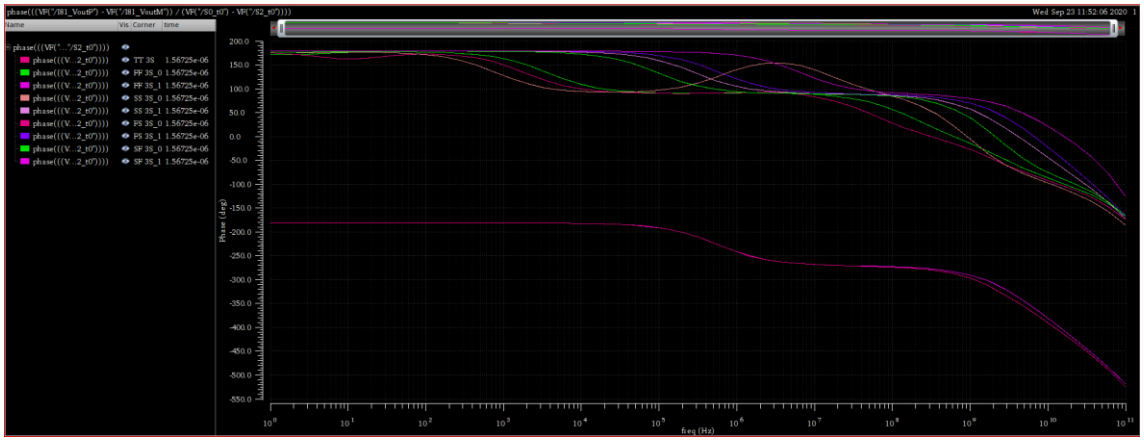

Figure 34 - Phase over corners of the steady state of the current starved ring amplifier.

The next table, Table 7, summarizes the results of the simulations for this ring amplifier. From these results and the figures above, it is possible to observe that this structure presents results much more viable than the one presented in section 6.1, however it still presents some variations over corners especially in the settling voltage and the time that some corners take to stabilize.

Table 7 - Simulation Results for CS FD.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
Gain (dB)	59.91	90.48	73.09	75.09	59.91	90.48	76.69	76.54	65.47	79.05	67.70
Loop Gain	-1.87	-1.66	-1.73	-1.86	-1.73	-1.72	-1.74	-1.66	-1.76	-1.87	-1.75
Settling Time (ps)	150	1348	630	1348	550	948.51	1150	150	416.28	240	470
V_{DZ} (mV)	512.44	690.77	554.80	600.57	512.44	631.44	554.04	690.77	605.06	687.79	600.67

The results for the FFT analysis over corners are presented in Figure 35 and Table 8. Similar to the transient and AC results, it doesn't show poor results, however, it still presents considerable variation over corners.

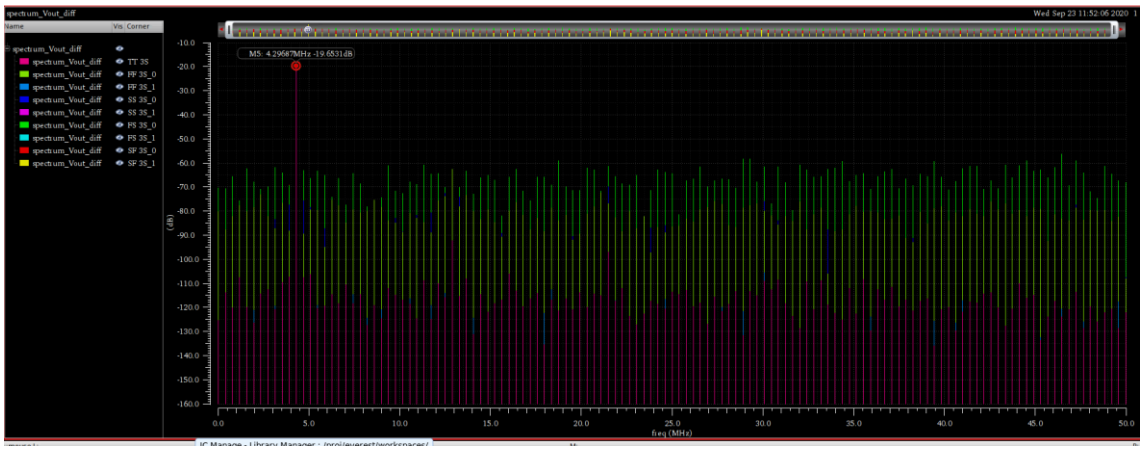

Figure 35 - FFT over corners of the current starved ring amplifier.

Table 8 - FFT values for CS FD without noise.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
SNR (dB)	22.86	78.91	73.40	39.36	78.91	43.05	72.79	22.86	70.61	42.42	73.08
SFDR (dB)	35.76	85.40	72.20	42.74	85.40	44.76	71.38	35.76	48	48.42	52.79
THDDB (dB)	-83.39	-37.31	-70.80	-42.25	-83.39	-43.25	-71.02	-37.31	-47.80	-44.37	-52.61
ENOB Equivalent (bits)	3.51	12.62	11.16	5.97	12.62	6.39	11.15	3.51	7.64	6.42	8.44

With the purpose of analyzing how the transient noise affects the response of the ringamp, the transient analysis, and the FFT analysis are repeated with transient noise, as explained in chapter 5. In Figure 36 is presented the transient response over corners with transient noise for this ring amplifier, and Figure 37 shows a close up of the previous figure.

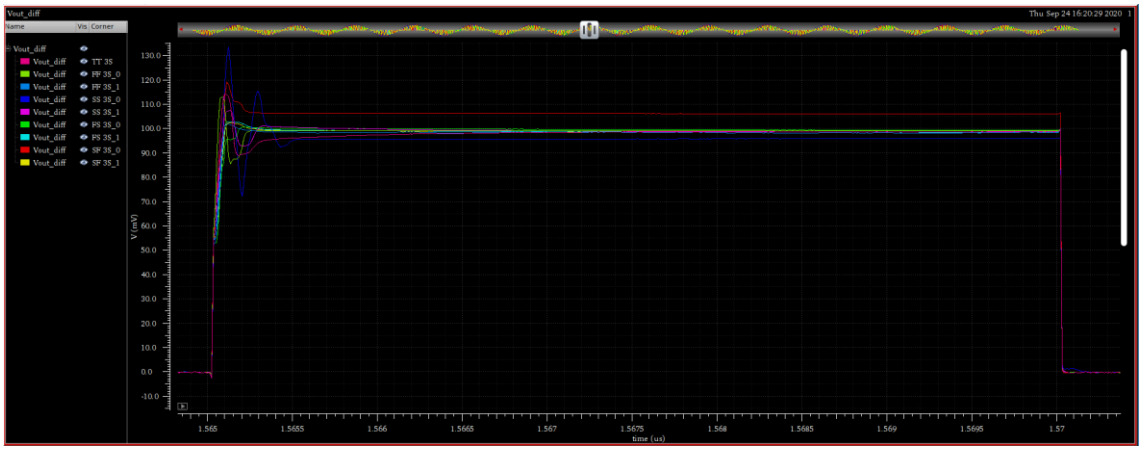

Figure 36 - Transient response over corners with transient noise of the current starved ring amplifier.

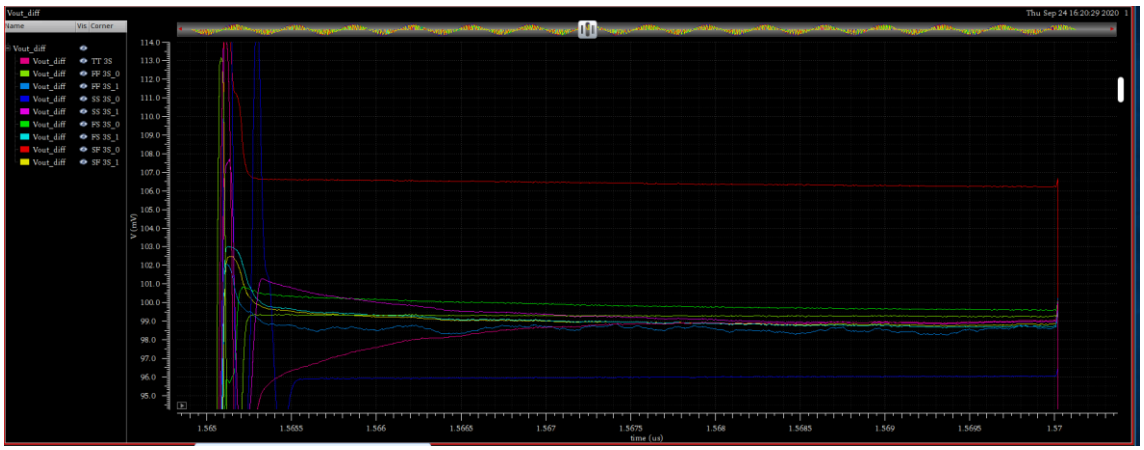

Figure 37 - Close in of transient response over corners with transient noise of the current starved ring amplifier.

Figure 38 presents the FFT with noise and Table 9 summarizes the important values from the FFT.

Figure 38 - FFT over corners with transient noise of the current starved ring amplifier.

Table 9 - FFT values for CS FD with worst case transient noise.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
SNR (dB)	23.02	42.56	41.80	37.20	40.18	36.02	42.33	23.02	41.64	39.35	42.56
SFDR (dB)	36.39	55.57	55.44	36.39	53.87	37.95	55.57	36.87	48.33	45.68	53.09
THDDB (dB)	-61.43	-36.18	-60.09	-36.18	-58.92	-37.34	-61.43	-40.85	-47.69	-44.20	-52.16
ENOB Equivalent (bits)	3.55	6.76	6.67	5.31	6.41	5.31	6.76	3.55	6.49	6.07	6.73

6.3 Proposed Topology - CMOS Resistor Fully Differential Ring Amplifier

Next is shown the simulation results for the proposed topology presented in Figure 20. In Appendix D, Figure 60 and Figure 61, is presented the Cadence Virtuoso schematic used for this simulation. Worth mentioning that the error amplifier was implemented using an ideal voltage-controlled current source for the same reasons as explained before, section 6.2.

Similar to both topologies already studied, Table 10 presents the values for the transistors multipliers and the current value for the current sources presented in the schematic. The devices in each stage are equal and represented in the table by the stage number. Devices MRN and MRP represent the transistors of the CMOS resistor. MBN and MFN are referring to the bottom transistors in the first stage. Gain error refers to the error amplifier gain and Gm error to the transconductance. Ibias2, Ibias3, and Ibias VBN present current values for the current sources in the biasing circuits. As explained in the previous section, these values are obtained after doing more than one iteration of the methodology presented in Figure 22, in order to reach the best response over corners.

Table 10 - Device Sizing for CMOS FD.

Global Variable	Stage 1	Stage 2	Stage 3	MRN MRP	MBN MFB	G error	Gm error	Ibias2	Ibias3	Ibias VBN
Value	75	10	2	1	75	30	10 mS	500 µA	250 µA	500 µA

When comparing Figure 39 with Figure 28, it is possible to observe that the corner variation is lesser than in the previous topology analyzed, both in the settling value and the settling time. As this topology is inspired in the same as the one used in the pseudo differential, it confirms the conclusion of the previous topology, that fully differential topologies present less variation over

corners than pseudo differential. However, it is possible to note that the corner FF 125°C still presents a slow response.

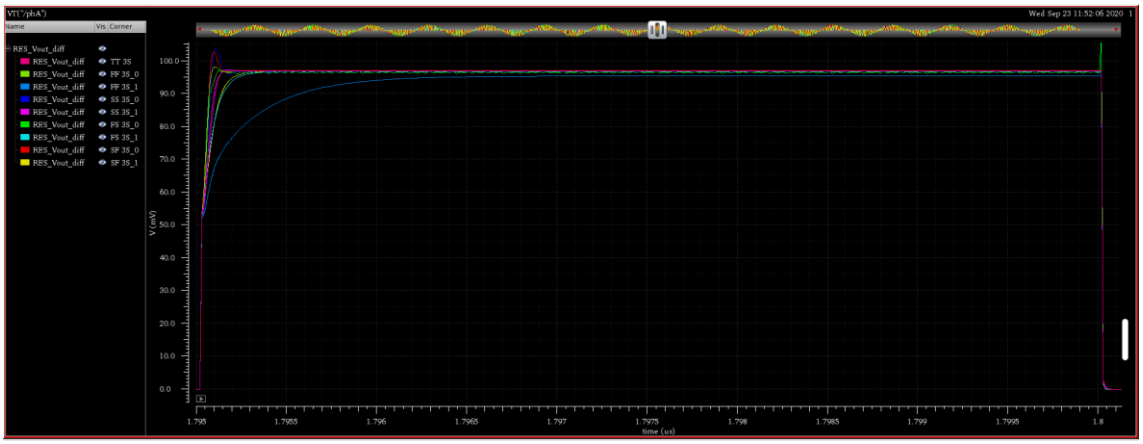

Figure 39 - Transient response over corners for FD CMOS Resistor.

In the next figure, Figure 40, is shown how the settling time was measured. The corner shown is the typical. In Table 11 is presented the settling time values for all corners.

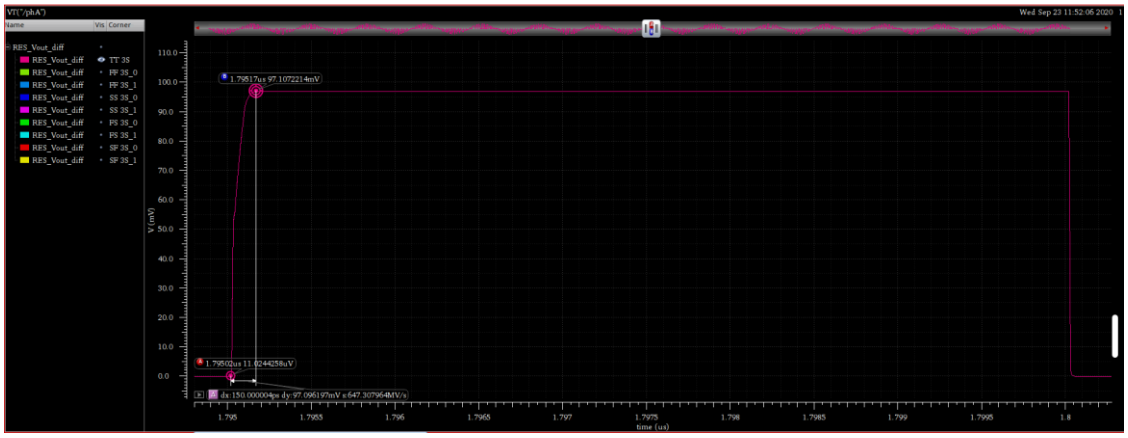

Figure 40 - Settling time measure for the typical corner of the CMOS resistor ring amplifier.

The times selected for the AC analysis are the same as the ones for the previous analysis, to allow a fair comparison between them. The mentioned times are represented in typical corner in Figure 41. However, as this ringamp is much faster, it does not have the oscillation phase, so there is no significant difference in the second and third AC analysis.

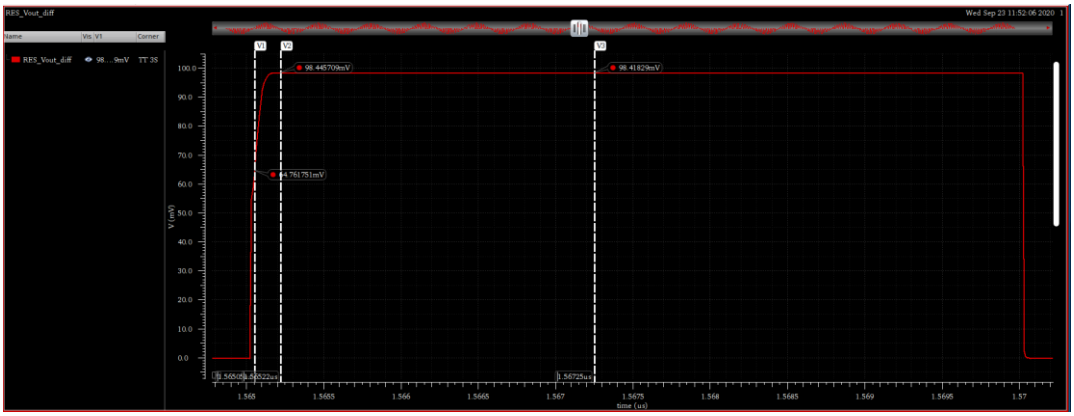

Figure 41 - The three selected times for the AC analysis in the three different phases for the FD CMOS Resistor ringamp: slewing, stabilization and steady state.

In Figure 42 and Figure 43 it is not possible to see the pole movement as clear as the previous topology because this structure settles much faster.

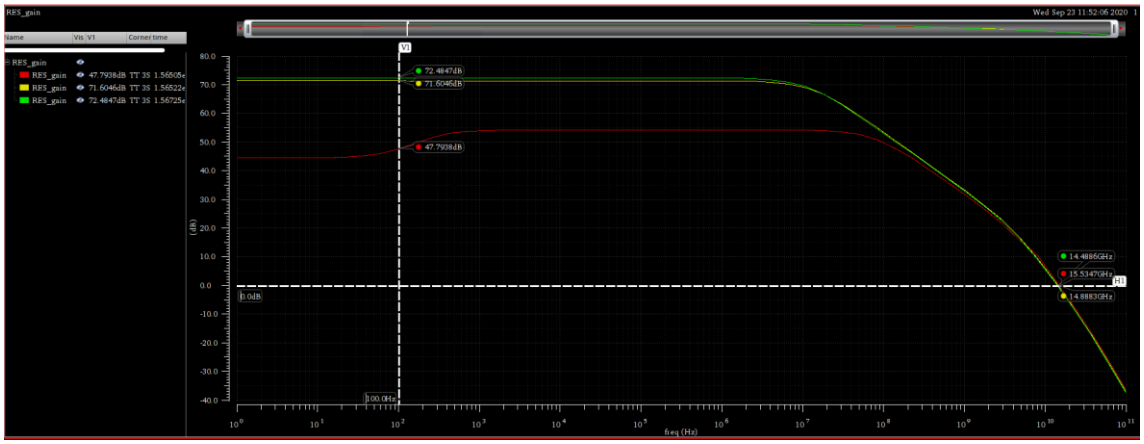

Figure 42 - Gain for each phase of operation for the Fully Differential CMOS Resistor Ring Amplifier. Red for slewing phase, yellow for stabilization phase and green for steady state.

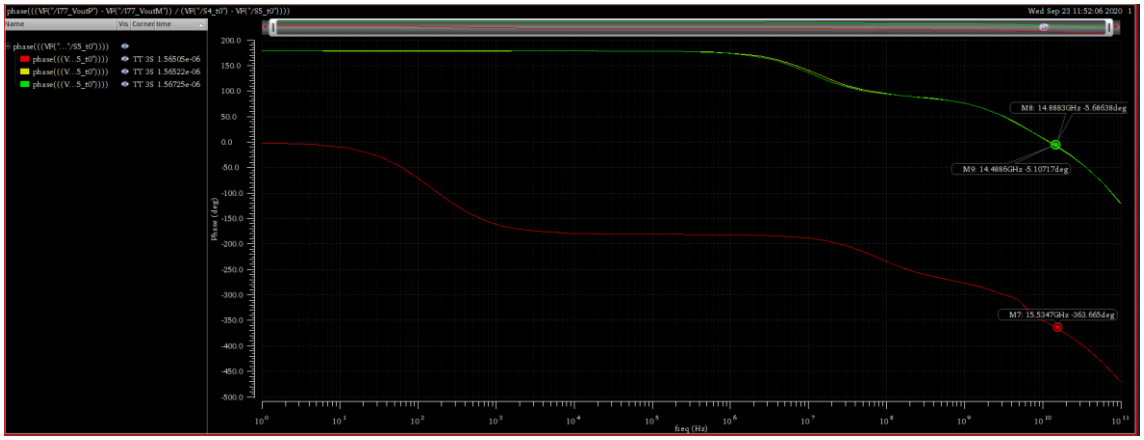

Figure 43 - Phase for each phase of operation for the Fully Differential CMOS Resistor Ring Amplifier. Red for slewing phase, yellow for stabilization phase and green for steady state.

The gain over corners in the steady state is represented in Figure 44. Despite the previous topology, this one presents a more linear response with higher bandwidth. Also presents a higher gain as can be seen in Table 11. Figure 45 completes the AC analysis in the steady state, presenting the phase over corners.

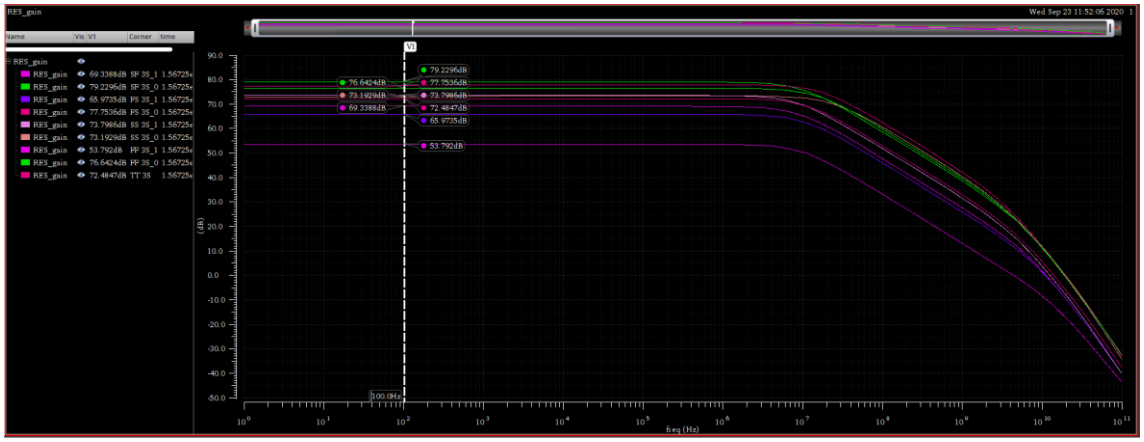

Figure 44 - Gain over corners for the Fully Differential CMOS Resistor Ring Amplifier.

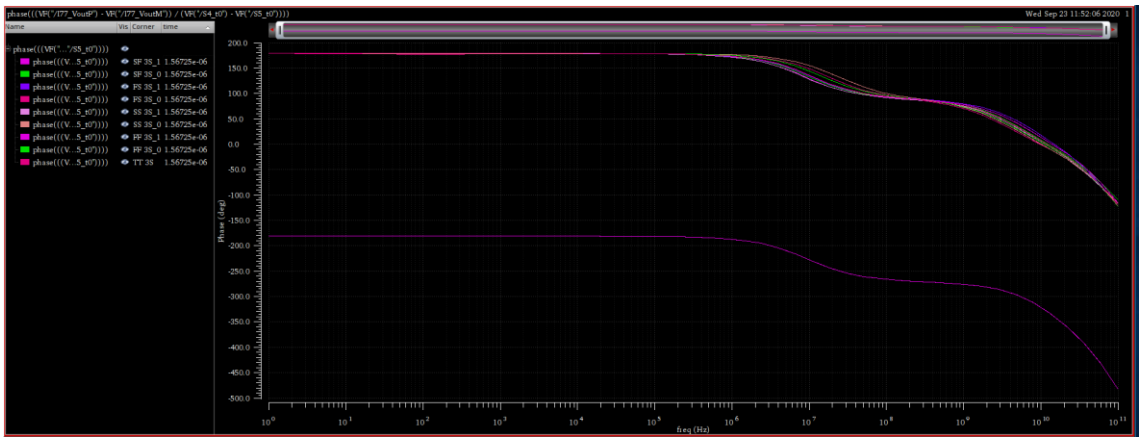

Figure 45 - Phase over corners for the Fully Differential CMOS Resistor Ring Amplifier.

The results for the AC and transient simulations over corners are summarized in Table 11. It is evident that the variation over corners is less significant, with the worst results focused on two corners, FF 125 °C being the slowest with less gain, and FS -40 °C presenting a very small variation, never being completely stable. The reason for the variation in these two corners can be explained in Figure 46, where it is possible to see the deadzone voltage. In the case of the corner FF 125 °C, it can be seen that it presents a V_{DZ} much higher than the rest, resulting in the mentioned slow response, and in the case of the corner FS -40 °C, a low value of V_{DZ}, not allowing the amplifier to stabilize.

Table 11 - Simulation Results for CMOS FD.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
Gain (dB)	53.79	79.23	72.48	76.64	53.79	73.19	73.80	77.75	65.97	79.23	69.34
Loop Gain	-1.74	-1.71	-1.74	-1.74	-1.71	-1.73	-1.74	-1.73	-1.73	-1.74	-1.73
Settling Time (ps)	150	1347.37	150	200	1347.37	280	230	-	403.82	397.10	450
V_{DZ} (mV)	84.93	466.40	267.59	281.96	466.40	84.93	204.76	163.47	306.83	165.95	307.61

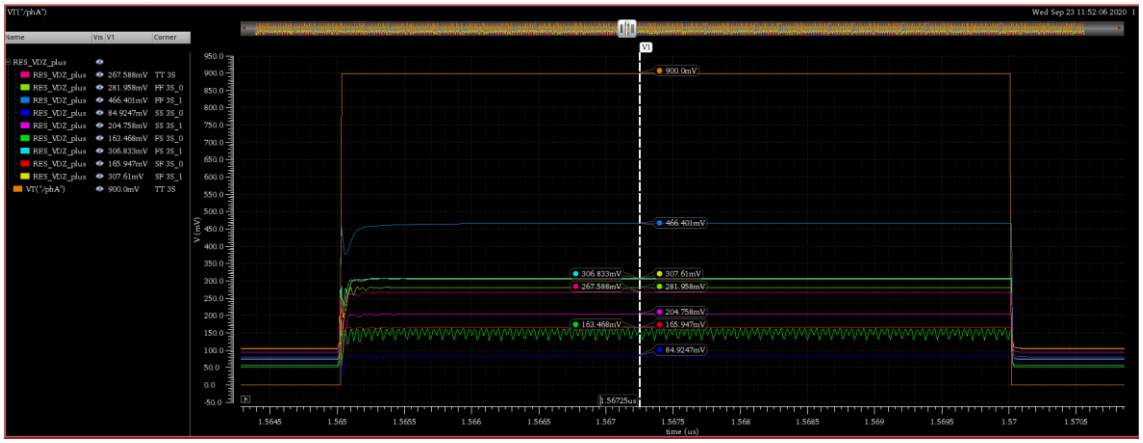

Figure 46 - Deadzone voltage over corners during the amplification phase for the Fully Differential CMOS Resistor Ring Amplifier.

The FFT results for the CMOS FD ringamp are presented in Figure 47 and Table 12 summarizes the important values of the FFT. It is clearly established that this structure presents much better results than the current starved FD topology because the variation over corners is lesser.

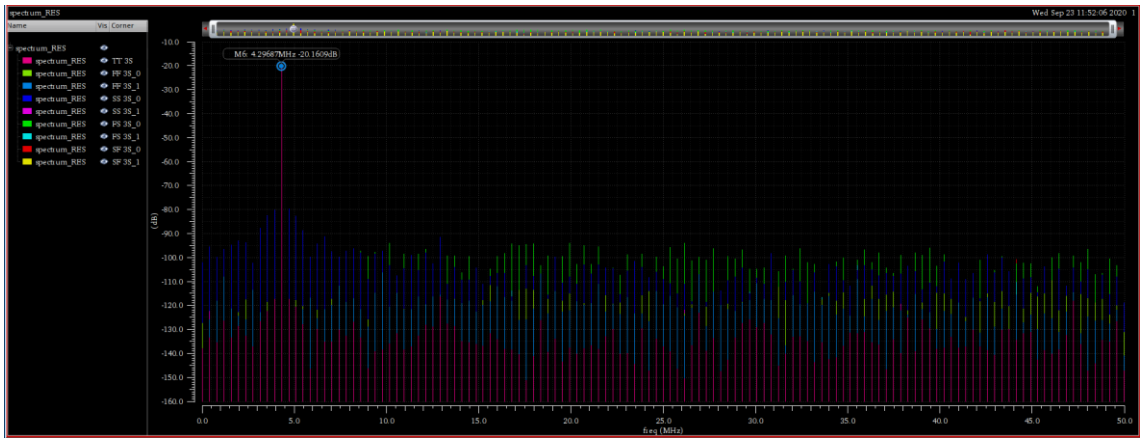

Figure 47 - FFT over corners for the Fully Differential CMOS Resistor Ring Amplifier.

Table 12 - FFT values for CMOS FD without noise.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
SNR (dB)	53.51	88.38	88.38	76.96	75.99	53.51	84.88	58.82	73.81	71.14	80.22
SFDR (dB)	59.61	96.28	96.28	89.42	86.14	59.61	95.02	72.99	83.15	80.58	86.26
THDDB (dB)	-95.94	-68.44	-95.94	-90.52	-86.63	-70.15	-93.05	-68.44	-87.04	-83.99	-86.09
ENOB Equivalent (bits)	8.61	14.30	14.30	12.49	12.30	8.61	13.73	9.43	11.97	11.52	12.89

Similar to the previous topology, with the purpose of analyzing how the transient noise affects the response of the ringamp, the transient analysis, and the FFT analysis are repeated with transient noise, as explained in chapter 5. In Figure 48 is presented the transient response over corners with transient noise and Figure 49 shows a close up of the settled value.

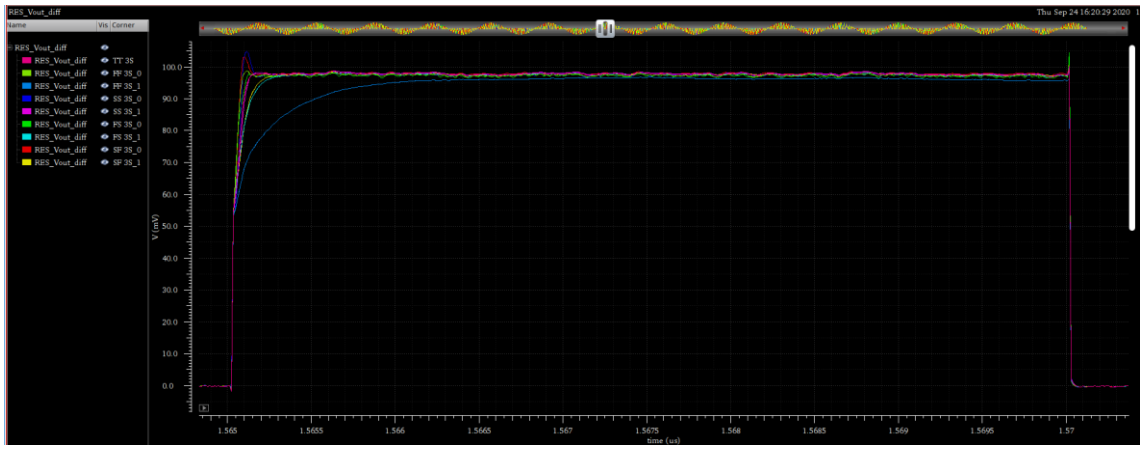

Figure 48 - Transient response over corners with transient noise for the Fully Differential CMOS Resistor Ring Amplifier.

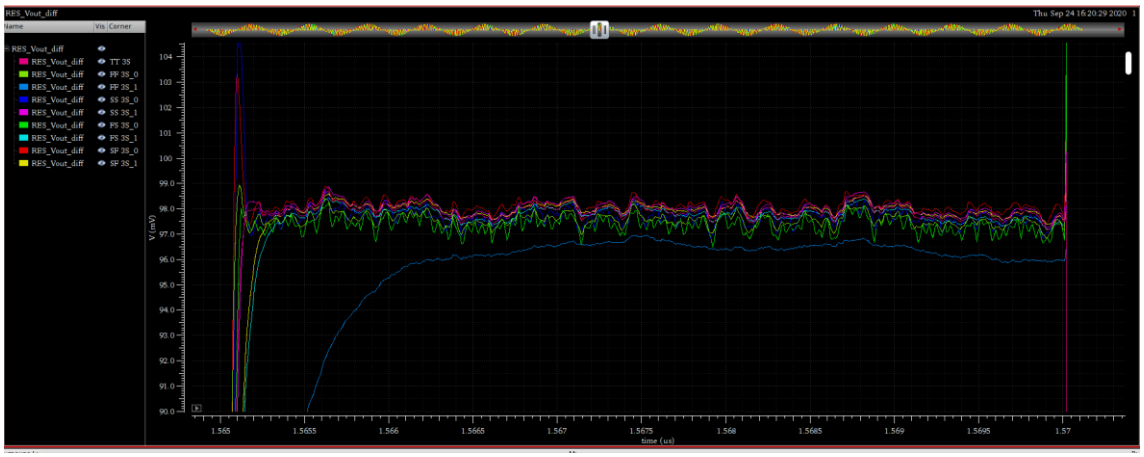

Figure 49 - Close up of transient response over corners with transient noise for the Fully Differential CMOS Resistor Ring Amplifier.

Figure 50 presents the FFT with noise and Table 13 summarizes the important values from the FFT. It is possible to observe that the variation over corners is not significant.

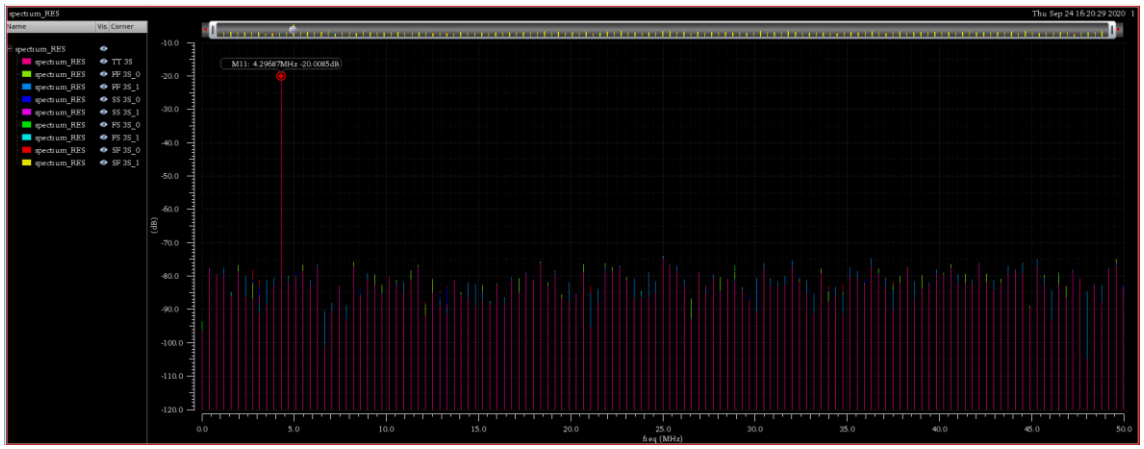

Figure 50 - FFT over corners with transient noise for the Fully Differential CMOS Resistor Ring Amplifier.

Table 13 - FFT values for CMOS FD with worst case transient noise.

	Min	Max	TT	FF 0	FF 1	SS 0	SS 1	FS 0	FS 1	SF 0	SF 1
SNR (dB)	39.54	41.52	40.21	39.59	39.54	41.26	40.48	40.47	40.14	41.52	41.05
SFDR (dB)	53.96	56.84	54.58	54.75	54.46	56.84	54.66	56.39	53.96	56.81	55.10
THDDB (dB)	-58.04	-53.62	-56.38	-55.31	-53.62	-57.30	-57.34	-57.57	-56.05	-58.04	-56.91
ENOB Equivalent (bits)	6.28	6.62	6.40	6.30	6.28	6.58	6.45	6.40	6.39	6.62	6.54

7. Conclusions and Future Perspectives

The main objective of this thesis was the study of ring amplifiers as an inverter-based amplifier, to serve as an alternative to conventional opamps in nanoscale technology. With this purpose in mind, and after a search in literature for the current solutions, a topology has been proposed merging some concepts present on the state of the art. The study was based on advanced CMOS FinFET 7 nm technology with XILINX parameterized cells with the focus of test functionality for industry use in this technology node. The main concern in industry use is to guarantee that the amplifier fulfills the specifications in all corners of process, temperature, and supply voltage variations.

Throughout the study, the proposed topology is compared with others presented in literature showing better results over corners and presenting a faster response. For this topology a gain of 72 dB was achieved for the typical corner and a range from 54 dB to 79 dB was obtained over PVT variations, with only one corner not fulfilling the initial specification, > 60 dB. For the settling time the specification was between 100 ps and 200 ps with the typical corner showing a settling time of 150 and a range from 150 ps to 403 ps over PVT variations. However, despite the promising results, the proposed topology isn't yet suitable for industry use, because it presents one corner significantly slower than the rest, with a settling time around 1347 ps, FF 125 °C, and the corner FS -40 °C with a small oscillation throughout the entire amplification period.

It is important to note that ring amplification is a very recent technique with room for further exploration, especially to solve the variability over corners for industry usage. One way to overcome this issue is to use different trimmings in each corner achieving the best behavior in each one. Another way to try to solve the variation problem is to explore more complex structures, like the one presented in [32] with second stage bias enhancement and deadzone degeneration as shown in Figure 51.

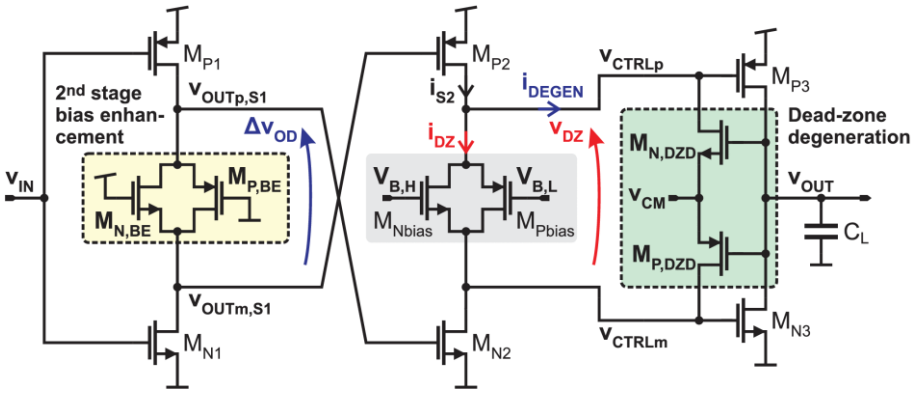

Figure 51 - Enhanced-linearity-and-BW ringamp featuring DZ and second-stage bias enhancement [32].

In [33] is explored a different concept combining high V_{Th} and low V_{Th} devices in the output stage in a dual-deadzone topology. However, to explore this kind of structure, the value of the supply voltage needs to be taken into consideration because the structure was explored in a 0.18 µm technology node and might not be viable in a 7 nm technology node. For further speed improvement without degrading the settling accuracy, the concept presented in [34] can be explored, the multi-path ring amplifier. When a structure with the desired behavior over corners is achieved, other considerations not approached in this work can be taken into account, such as power dissipation with several power down techniques presented in literature, using enable in the different stages, and switching down the CMOS resistor during the sampling phase.

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Appendix A – Schematics for Fully Differential Testbench

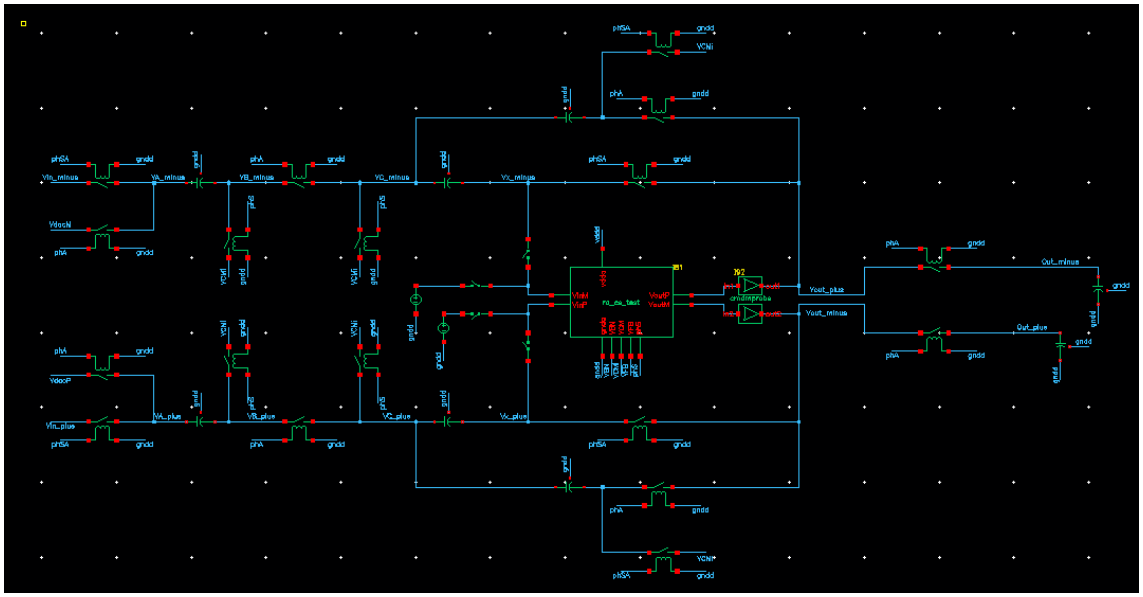

Figure 52 - Testbench for the fully-differential topology.

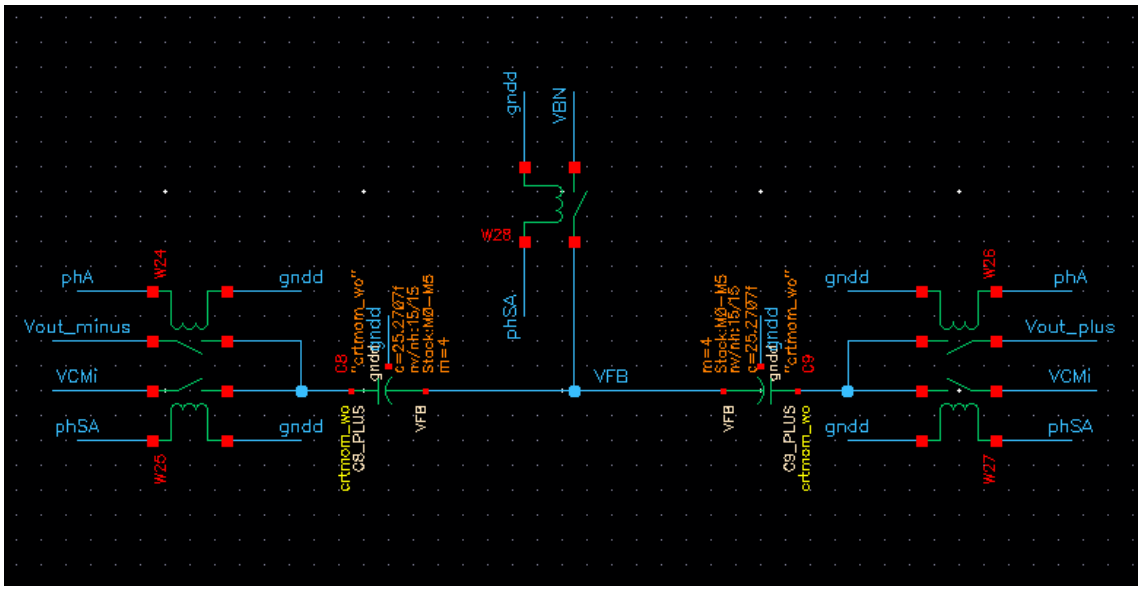

Figure 53 - Common mode feedback circuit.

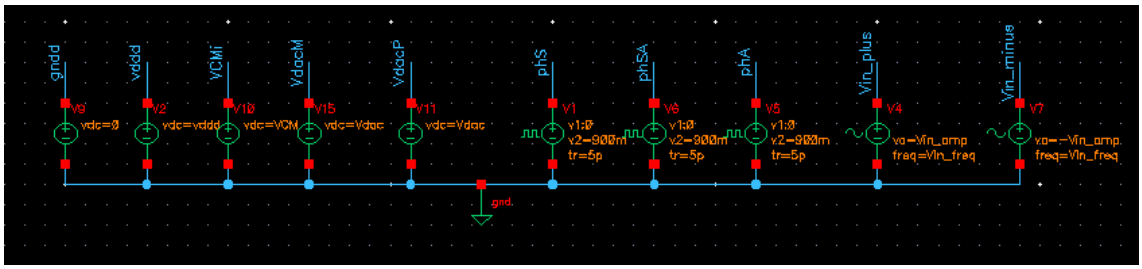

Figure 54 - Ideal voltage sources for DC voltages, clock signal, and input signal.

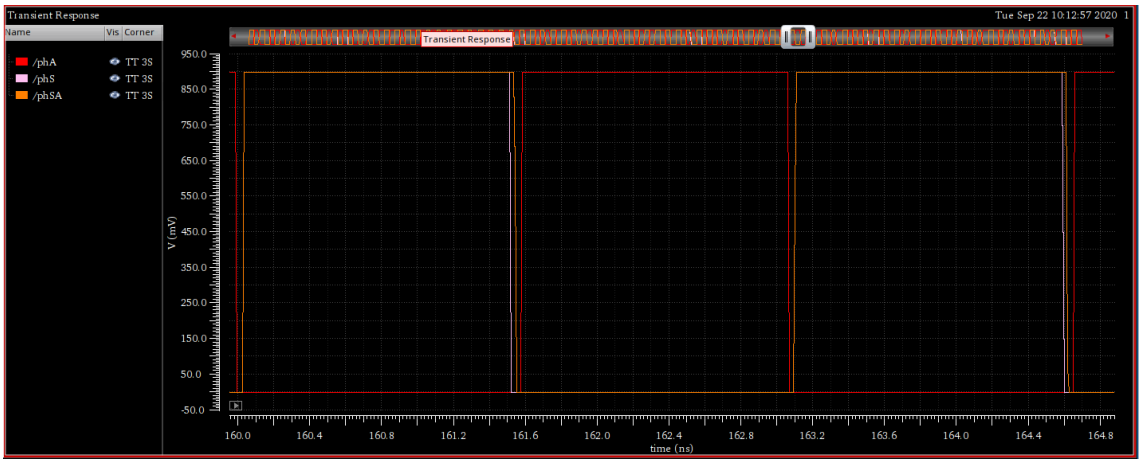

Figure 55 - Clock signals over time.

Appendix B – Schematics for Pseudo Differential

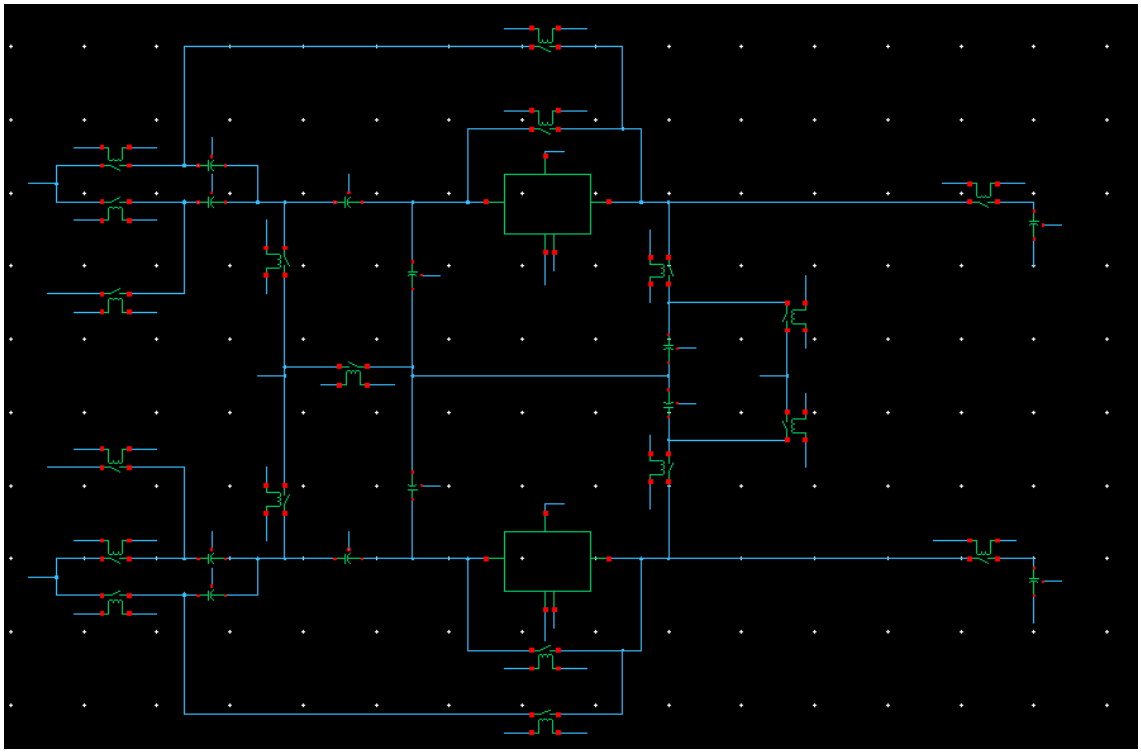

Figure 56 - Testbench for PD topology.

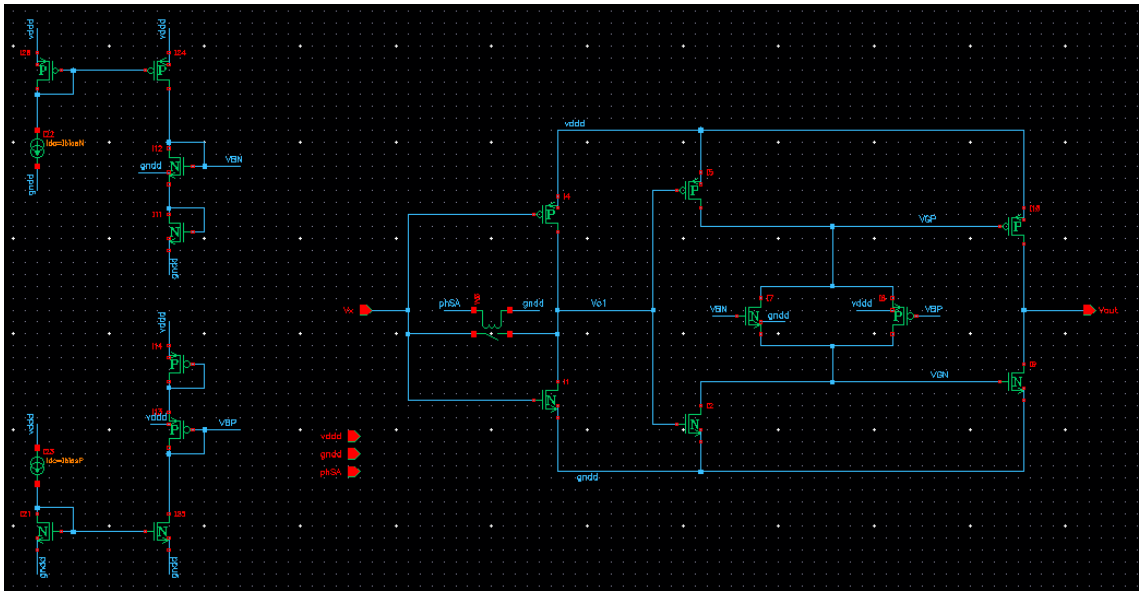

Figure 57 - Schematic for the CMOS Resistor topology on the left. On the right the biasing circuit for the CMOS resistor.

Appendix C – Cadence Virtuoso Schematics for Current Starved Ring Amplifier

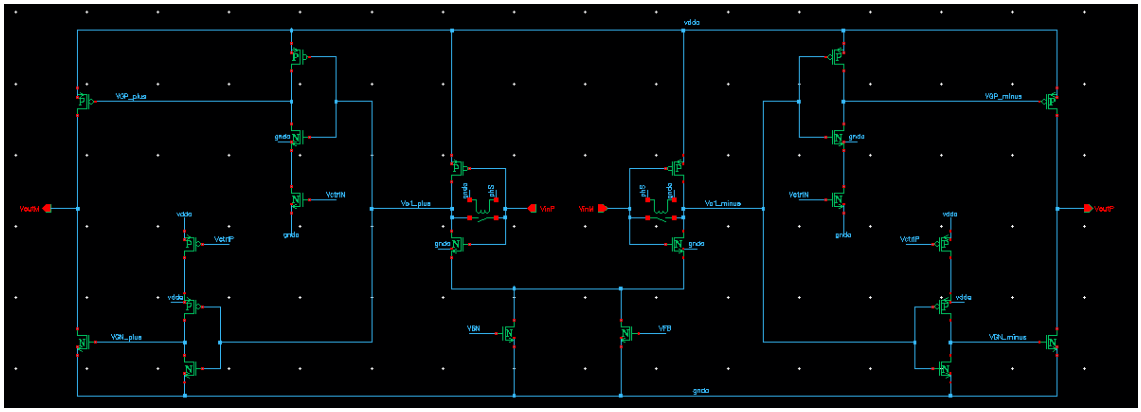

Figure 58 – Cadence Virtuoso schematic for the Fully-Differential Current Starved Ring Amplifier.

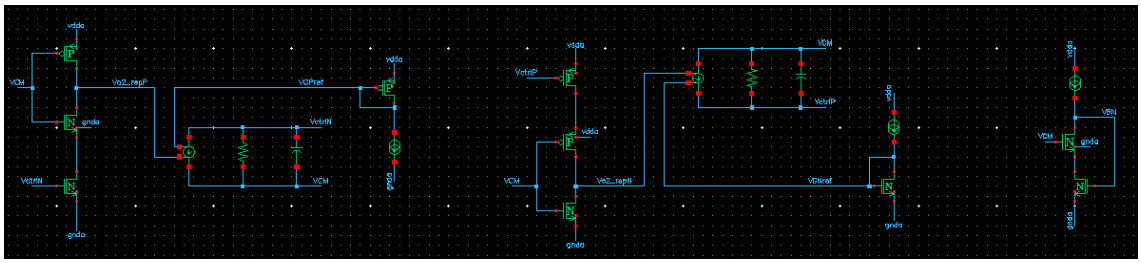

Figure 59 – Cadence Virtuoso schematic of the biasing circuits for the NMOS and PMOS devices of the Current Starved stage, respectively. On the right the biasing circuit for the V_{BN} device.

Appendix D – Cadence Virtuoso Schematic for Proposed Topology

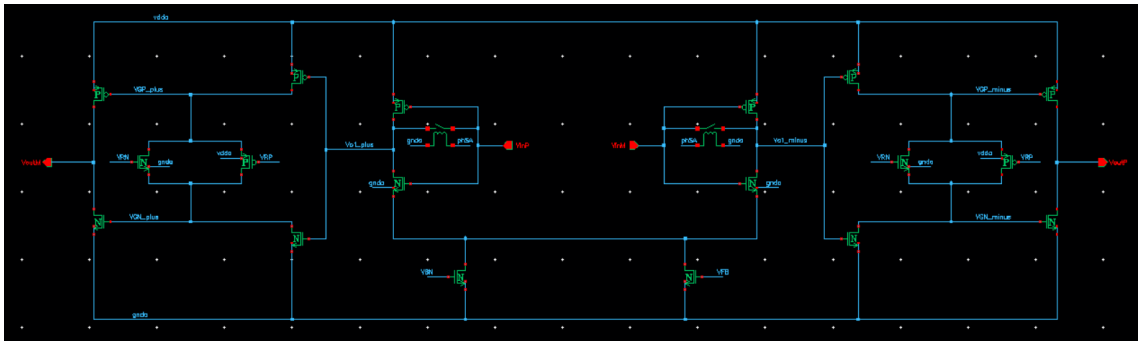

Figure 60 – Cadence virtuoso schematic for the Fully-Differential CMOS Resistor Ring Amplifier.

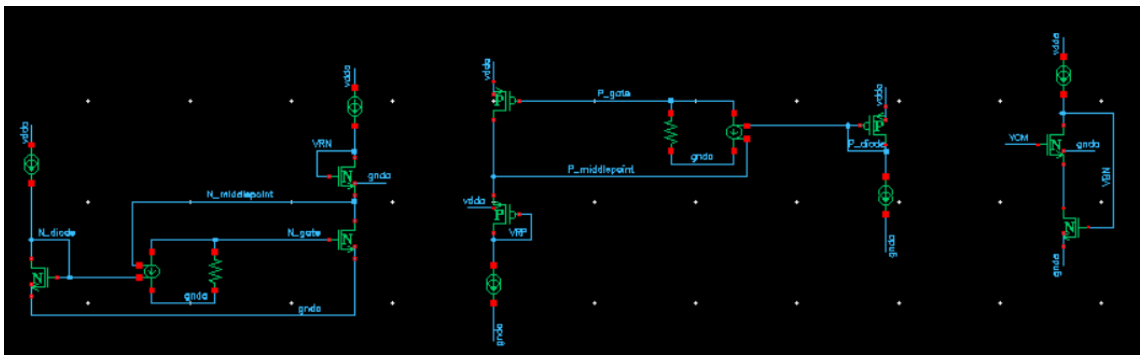

Figure 61 - Biasing circuits for the NMOS and PMOS devices of the CMOS Resistor, respectively. On the right the biasing circuit for the V_{BN} device.